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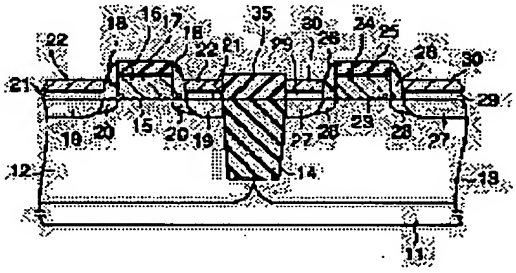
(54) SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To increase the degree of integration of a semiconductor device by restricting the horizontal growth of an epitaxial layer.
SOLUTION: In a semiconductor device, an element isolation insulating film 14 constituted in an STI structure is arranged between two MOSFETs. The surface of the insulating film 14 is substantially equal to that of a silicon substrate 11. On the insulating film 14, a stopper insulating film 35, having a width which is equal to or narrower than that of the insulating film 14, is arranged. Each MOSFET has an elevated source/drain structure, and the surfaces of epitaxial layers 21 and 29 which function as source/drain regions are positioned higher than the channel of each MOSFET. When the epitaxial layers 21 and 29 are selectively grown, the horizontal growth of the layers 21 and 29 is restricted by the stopper insulating film 35 which works as a wall.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention is used for MISFET which has the EREBETEDDO source / drain (elevated source/drain) structure, concerning the semiconductor device which has the epitaxial layer alternatively formed on a semi-conductor substrate.
[0002]
[Description of the Prior Art] (1) The so-called EREBETEDDO source / drain structure are conventionally proposed for the purpose of the improvement in the engine performance of MISFET (generally MOSFET). The EREBETEDDO source / drain structure is structures which have arranged the front face of the source / drain field in the location higher than the front face (channel of MOSFET) of a silicon substrate.
[0003] Drawing 54 shows the conventional CMOS integrated circuit which consists of MOSFETs which have the EREBETEDDO source / drain structure.
[0004] In the single crystal silicon substrate 11, p mold well field 12 and n mold well field 13 are formed. A silicon substrate 11 may be n mold, or may be p mold. Between p mold well field 12 and n mold well field 13, the isolation insulator layer 14 of STI (shallow trenchisolation) structure is formed.
[0005] Here, the front face of a silicon substrate 11 and the front face of the isolation insulator layer 14 are in agreement in general. If the front face of the isolation insulator layer 14 is made in agreement with the front face of a silicon substrate 11, it will be because processing of the gate electrode formed ranging over a silicon substrate 11 and the isolation insulator layer 14 can carry out easily for example.
[0006] The n channel mold MOSFET is formed on p mold well field 12.
[0007] That is, on p mold well field 12, the polish recon film (gate electrode) 16 containing silicon oxide (gate dielectric film) 15 and an impurity is formed. On the polish recon film 16, the silicon oxide (cap oxide film) 17 used as the mask at the time of processing the polish recon film 16 is formed. Moreover, the silicon nitride (side-attachment-wall insulator layer) 18 is formed in the side attachment wall of the polish recon film 16.
[0008] In p mold well field 12, low-concentration n mold extension field 20 is formed rather than n mold source / drain field 19, and this the source / drain field 19. That is, the source / drain field 19 is formed in p mold well field 12 of the both sides of the polish recon film 16, and n mold extension field 20 is formed in p mold well field [directly under] 12 of the silicon nitride 18.
[0009] On a silicon substrate 11 (the source / drain field 19), an epitaxial layer 21 is formed alternatively. Since an epitaxial layer 21 consists of single crystal silicon and contains the impurity of n mold like the silicon substrate 11 (the source / drain field 19), it has become a part of source / drain field 19.
[0010] On an epitaxial layer (the source / drain field) 21, the refractory metal silicide layers (a tungsten silicide layer, titanium silicide layer, etc.) 22 are formed. In this example, although the refractory metal silicide layer 22 is not formed on the polish recon film (gate electrode) 16, it may remove silicon oxide (cap oxide film) 17, and may form it on the polish recon film 16 (Salicide structure).
[0011] The p channel mold MOSFET is formed on n mold well field 13.
[0012] That is, on n mold well field 13, the polish recon film (gate electrode) 24 containing silicon oxide (gate dielectric film) 23 and an impurity is formed. On the polish recon film 24, the silicon oxide (cap oxide film) 25 used as the mask at the time of processing the polish recon film 24 is formed. Moreover, the silicon nitride (side-attachment-wall insulator layer) 26 is formed in the side attachment wall of the polish recon film 24.
[0013] In n mold well field 13, low-concentration p mold extension field 28 is formed rather than p mold source / drain field 27, and this the source / drain field 27. That is, the source / drain field 27 is formed in n mold well field 13 of the

both sides of the polish recon film 24, and p mold extension field 28 is formed in n mold well field [directly under] 13 of the silicon nitride 26.
[0014] On a silicon substrate 11 (the source / drain field 27), an epitaxial layer 29 is formed alternatively. Since an epitaxial layer 29 consists of single crystal silicon and contains the impurity of p mold like the silicon substrate 11 (the source / drain field 27), it has become a part of source / drain field 27.
[0015] On an epitaxial layer (the source / drain field) 29, the refractory metal silicide layers (a tungsten silicide layer, titanium silicide layer, etc.) 30 are formed. In this example, although the refractory metal silicide layer 30 is not formed on the polish recon film (gate electrode) 24, it may remove silicon oxide (cap oxide film) 25, and may form it on the polish recon film 24 (Salicide structure).
[0016] As an interlayer insulation film 31 covers completely an n channel mold MOS transistor and a p channel mold MOS transistor, it is formed on a silicon substrate 11. An interlayer insulation film 31 consists of silicon oxide. The contact hole which reaches the polish recon film (gate electrode) 16 and the refractory metal silicide layer 22 is established in an interlayer insulation film 31.
[0017] The contact plugs 32a and 32b which consist of conductive ingredients (a metal, refractory metal silicide, etc.) are embedded in a contact hole. Moreover, Wiring 33a and 33b is formed on an interlayer insulation film 31, and the end is connected to the contact plugs 32a and 32b.
[0018] On an interlayer insulation film 31, the passivation film 34 which covers Wiring 33a and 33b is formed. The passivation film 34 consists of insulator layers, such as a silicon nitride.
[0019] Next, the manufacture approach of an above-mentioned CMOS integrated circuit is explained.
[0020] First, as shown in drawing 55 , the isolation insulator layer 14 of STI structure is formed in the single crystal silicon substrate 11.
[0021] The isolation insulator layer 14 is formed by grinding and etching silicon oxide by CMP (chemical mechanical polishing), after using for example, a silicon nitride as a mask, forming a trench in a silicon substrate and forming the silicon oxide which fills the inside of a trench completely on a silicon nitride.
[0022] A silicon nitride functions as a stopper at the time of CMP, and after a CMP process is completed, it is removed.

[0023] In addition, what is necessary is to carry out over etching of the silicon oxide for example, at the time of CMP, or just to etch silicon oxide further by the option after CMP, in order to make the front face of the isolation insulator layer 14 in general equal to the front face of a silicon substrate 11.
[0024] Next, as shown in drawing 56 , with ion-implantation, in a silicon substrate 11, the ion implantation of the p mold impurity is carried out, p mold well field 12 is formed, and in a silicon substrate 11, the ion implantation of the n mold impurity is carried out, and n mold well field 13 is formed. Then, for example, silicon oxide (gate oxide) 15 and 23 is formed on the component field enclosed by the isolation insulator layer 14 by the oxidizing [thermally] method.
[0025] For example, the isolation insulator layer 14 top and silicon oxide 15, and the polish recon film 16 and 24 that contained the impurity on 23 are formed using a CVD method. Silicon oxide (cap oxide film) 17 and 25 is formed on the polish recon film 16 and 24 with a CVD method continuing. Then, PEP (photo-etching process) is performed and silicon oxide 17 and the resist film which has a predetermined pattern on 25 are formed.
[0026] This resist film is used as a mask and silicon oxide 17 and 25 is etched by RIE. Then, the resist film exfoliates. Moreover, silicon oxide 17 and 25 is used as a mask, and the polish recon film 16 and 24 is etched by RIE. Consequently, the gate electrode of MOSFET which consists of polish recon film 16 and 24 is done.
[0027] Then, even if it removes, it is not necessary to remove silicon oxide 17 and 25. In this example, silicon oxide 17 and 25 is made to leave as it is.
[0028] Moreover, using ion-implantation, the polish recon film (gate electrode) 16 is used as a mask, and the ion implantation of the n mold impurity is carried out into p mold well field 12 by the self aryne. Consequently, in p mold well field 12, shallow and low-concentration n mold impurity range 20, i.e., n mold extension field, is formed.
[0029] Similarly, using ion-implantation, the polish recon film (gate electrode) 24 is used as a mask, and the ion implantation of the p mold impurity is carried out into n mold well field 13 by the self aryne. Consequently, in n mold well field 13, shallow and low-concentration p mold impurity range 28, i.e., p mold extension field, is formed.
[0030] Then, it oxidizes thermally and silicon oxide is formed in the front face of the polish recon film (gate electrode) 16 and 24.
[0031] Moreover, for example, the silicon nitrides 18 and 26 which cover completely the polish recon film (gate electrode) 16 and 24 on [whole] the isolation insulator layer 14 and a component field are formed with a CVD method. Moreover, the silicon nitrides 18 and 26 are etched and these silicon nitrides 18 and 26 are made to remain only on the side attachment wall of the polish recon film 16 and 24 by RIE.

[0032] Then, the silicon oxide 15 and 23 of the both sides of the polish recon film 16 and 24 is removed, and a silicon substrate 11 20, i.e., n mold extension field, and p mold extension field 28 are exposed.
[0033] Next, as shown in drawing 57 , while forming alternatively an epitaxial layer (single-crystal-silicon layer) 21 with selection epitaxial growth on n mold extension field 20 (silicon substrate 11) which became unreserved, an epitaxial layer (single-crystal-silicon layer) 29 is alternatively formed on p mold extension field 28 (silicon substrate 11) which became unreserved.
[0034] in addition, the thing for which material gas, membrane formation temperature, etc. are adjusted with a selection epitaxial grown method -- being alternative (for example, only in case of on silicon) -- it is the thing of the technique which forms an epitaxial layer.
[0035] In this example, since silicon oxide 17 and 25 exists on the polish recon film 16 and 24, an epitaxial layer does not grow on the polish recon film 16 and 24. However, in removing silicon oxide 17 and 25 beforehand, on the polish recon film 16 and 24, a polish recon epitaxial layer grows at the time of selection epitaxial growth.
[0036] Next, as shown in drawing 58 , using ion-implantation, the polish recon film 16 and the silicon nitride 18 are used as a mask, and the ion implantation of the n mold impurity is carried out into p mold well field 12 and an epitaxial layer 21 by the self aryne. Moreover, using ion-implantation, the polish recon film 24 and the silicon nitride 26 are used as a mask, and the ion implantation of the p mold impurity is carried out into n mold well field 13 and an epitaxial layer 29 by the self aryne.
[0037] Consequently, in p mold well field 12 and an epitaxial layer 21, the high-concentration impurity range 19 deeper than n mold extension field 20 and, i.e., n mold source / drain field, is formed, and the high-concentration impurity range 27 deeper than p mold extension field 28 and, i.e., p mold source / drain field, is formed in n mold well field 13 and an epitaxial layer 29.
[0038] Moreover, for example, refractory metal film (a tungsten, titanium, etc.) is formed with a CVD method on an epitaxial layer 21 and the whole surface of the silicon substrate 11 including 29 tops. Then, if annealing is performed (like a heat process), an epitaxial layer 21, and the silicon and the refractory metal film in 29 will react chemically, and the refractory metal silicide layers 22 and 30 will be formed in the upper part of epitaxial layers 21 and 29.
[0039] Then, the unreacted refractory metal film is removed.
[0040] Here, when removing beforehand the polish recon film (gate electrode) 16 and the silicon oxide 17 and 25 on 24, at the time of annealing, the polish recon film 16 and 24 and the refractory metal film react chemically, and a refractory metal silicide layer is formed also in the upper part of the polish recon film 16 and 24 (Salicide structure).
[0041] Next, as shown in drawing 59 , an interlayer insulation film 31 is formed on [whole] a silicon substrate 11 with a CVD method. Moreover, the contact hole which reaches the contact hole and the refractory metal silicide layer 22 which reach an interlayer insulation film 31 at the polish recon film 16, for example using PEP and an etching technique is formed.
[0042] Moreover, for example, the contact plugs 32a and 32b are formed in these contact holes using CVD and a CMP technique. Then, Wiring 33a and 33b is formed on an interlayer insulation film 31. Finally, the passivation film 34 is formed on an interlayer insulation film 31 with a CVD method.
[0043] The CMOS integrated circuit constituted from an MOSFET which has the EREBETEDDO source / drain structure by the above process is completed.
[0044] Next, the advantage of the EREBETEDDO source / drain structure is explained.
[0045] Drawing 60 shows the structure of the usual MOSFET which does not have the EREBETEDDO source / drain structure. Drawing 61 shows the structure of MOSFET which has the EREBETEDDO source / drain structure.
[0046] As shown in drawing 60 , in order to reduce parasitism resistance, generally by the usual MOSFET, the silicide layer 22 of low resistance is formed on the source / drain field 19. This silicide layer 22 is formed of the chemical reaction of the source / drain field (silicon substrate) 19, and the refractory metal film. For this reason, the silicide layer 22 is formed in the source / drain field 19.
[0047] However, if the silicide layer 22 advances too much into the source / drain field 19, the silicide layer 22 will contact the depletion layer generated in a junction interface (junction interface of the well field 12, and the source / drain field 19), or its near, and will cause leakage current and a poor proof pressure.
[0048] Therefore, in the usual MOSFET, the depth xj1 (equal to the distance xj2 from a channel (substrate front face) to a junction interface) of the source / drain field 19 was set up greatly (for example, xj=0.15-0.1micrometer), and it has prevented leakage current and the poor proof pressure of the silicide layer 22 by penetration.
[0049] However, if the depth xj1 of the source / drain field 19 becomes large and the distance xj2 from a channel (substrate front face) to a junction interface becomes large, it will become easy to generate the short channel effect. Moreover, although the short channel effect can be controlled by making concentration of the well field 12 high, on the

other hand, the threshold of MOSFET becomes high or the problem of parasitic capacitance increasing arises.
[0050] On the other hand, in MOSFET which has the EREBETEDDO source / drain structure, as shown in drawing 61 , since an epitaxial layer 21 also functions as a part of source / drain field 19, the depth xj1 of the source / drain field can be enlarged enough. For this reason, the problem of the leakage current by the silicide layer 22 or a poor proof pressure is avoidable.
[0051] Moreover, the distance xj2 from a channel (substrate front face) to a junction interface can be set up smaller than the depth xj1 of the source / drain field. For this reason, the short channel effect can be controlled.
[0052] Next, reduction of the parasitic capacitance of MOSFET is considered.
[0053] As shown in drawing 62 , in the case of the usual MOSFET, the parasitic capacitance between the well field 12, and the source / drain field 19 makes the source / drain field 19 small, namely, can reduce it by making small area of the junction interface of the well field 12, and the source / drain field 19.
[0054] However, the contact field to wiring is prepared on the source / drain field 19. Since it is unreducible, in fact, this contact field cannot make the source / drain field 19 small, but has the problem which cannot fully perform reduction of parasitic capacitance.
[0055] On the other hand, as shown in drawing 63 , in MOSFET which has the EREBETEDDO source / drain structure, the contact field to the source / drain field is prepared on the epitaxial layer 21 on the component demarcation membrane 14. For this reason, regardless of a contact field, the source / drain field 19 in a silicon substrate 11 are made small, namely, it is possible to make small area of the junction interface of the well field 12, and the source / drain field 19, and sharp reduction of parasitic capacitance is possible.
[0056] (2) Conventionally, MISFET (generally MOSFET) is formed in an epitaxial layer, and the structure of attaining the improvement in the engine performance of MISFET is proposed.
[0057] Drawing 64 shows the conventional CMOS integrated circuit which consists of MOSFETs formed in the epitaxial layer.
[0058] Epitaxial layers 21 and 29 are formed on the single crystal silicon substrate 11. Epitaxial layers 21 and 29 consist of single crystal silicon like a silicon substrate 11. p mold well field 12 is formed in a silicon substrate 11 and an epitaxial layer 21, and n mold well field 13 is formed in a silicon substrate 11 and an epitaxial layer 29.
[0059] A silicon substrate 11 may be n mold, or may be p mold. Between p mold well field 12 and n mold well field 13, the isolation insulator layer 14 of STI structure is formed. The front face of a silicon substrate 11 and the front face of the isolation insulator layer 14 are in agreement in general.
[0060] The n channel mold MOSFET is formed on p mold well field 12.
[0061] That is, on p mold well field 12, the polish recon film (gate electrode) 16 containing silicon oxide (gate dielectric film) 15 and an impurity is formed. On the polish recon film 16, the silicon oxide (cap oxide film) 17 used as the mask at the time of processing the polish recon film 16 is formed. Moreover, the silicon nitride (side-attachment-wall insulator layer) 18 is formed in the side attachment wall of the polish recon film 16.
[0062] In p mold well field 12, low-concentration n mold extension field 20 is formed rather than n mold source / drain field 19, and this the source / drain field 19. That is, the source / drain field 19 is formed in p mold well field 12 of the both sides of the polish recon film 16, and n mold extension field 20 is formed in p mold well field [directly under] 12 of the silicon nitride 18.
[0063] A part of source / drain field 19 exist on the isolation insulator layer 14. For this reason, since the area of the junction interface of p mold well field 12, and the n mold source / drain field 19 becomes small, parasitic capacitance in the source / drain field 19 can be made small. Moreover, since the epitaxial layer 21 on the isolation insulator layer 14 also functions as the source / a drain field, a contact field is also securable.
[0064] The p channel mold MOSFET is formed on n mold well field 13.
[0065] That is, on n mold well field 13, the polish recon film (gate electrode) 24 containing silicon oxide (gate dielectric film) 23 and an impurity is formed. On the polish recon film 24, the silicon oxide (cap oxide film) 25 used as the mask at the time of processing the polish recon film 24 is formed. Moreover, the silicon nitride (side-attachment-wall insulator layer) 26 is formed in the side attachment wall of the polish recon film 24.
[0066] In n mold well field 13, low-concentration p mold extension field 28 is formed rather than p mold source / drain field 27, and this the source / drain field 27. That is, the source / drain field 27 is formed in n mold well field 13 of the both sides of the polish recon film 24, and p mold extension field 28 is formed in n mold well field [directly under] 13 of the silicon nitride 26.
[0067] A part of base of the source / drain field 27 touches the isolation insulator layer 14. For this reason, since area of the junction interface of n mold well field 13, and the p mold source / drain field 27 can be made small, parasitic capacitance in the source / drain field 27 can be made small. Moreover, since the epitaxial layer 29 on the isolation

insulator layer 14 also functions as the source / a drain field, a contact field is also securable.
[0068] As an interlayer insulation film 31 covers completely an n channel mold MOS transistor and a p channel mold MOS transistor, it is formed on a silicon substrate 11. An interlayer insulation film 31 consists of silicon oxide. The contact hole which arrives at the polish recon film (gate electrode) 16, and the n mold source / drain field 19 is established in an interlayer insulation film 31.
[0069] The contact plugs 32a and 32b which consist of conductive ingredients (a metal, refractory metal silicide, etc.) are embedded in a contact hole. Moreover, Wiring 33a and 33b is formed on an interlayer insulation film 31, and the end is connected to the contact plugs 32a and 32b.
[0070] On an interlayer insulation film 31, the passivation film 34 which covers Wiring 33a and 33b is formed. The passivation film 34 consists of insulator layers, such as a silicon nitride.
[0071] Next, the manufacture approach of an above-mentioned CMOS integrated circuit is explained.
[0072] First, as shown in drawing 65 , the isolation insulator layer 14 of STI structure is formed in the single crystal silicon substrate 11.
[0073] The isolation insulator layer 14 is formed by grinding and etching silicon oxide by CMP, after using for example, a silicon nitride as a mask, forming a trench in a silicon substrate and forming the silicon oxide which fills the inside of a trench completely on a silicon nitride.
[0074] A silicon nitride functions as a stopper at the time of CMP, and after a CMP process is completed, it is removed.

[0075] In addition, what is necessary is to carry out over etching of the silicon oxide for example, at the time of CMP, or just to etch silicon oxide further by the option after CMP, in order to make the front face of the isolation insulator layer 14 in general equal to the front face of a silicon substrate 11.
[0076] Next, as shown in drawing 66 , epitaxial layers (single-crystal-silicon layer) 21 and 29 are alternatively formed on a silicon substrate 11 with a selection epitaxial grown method. In this selection epitaxial growth, an epitaxial layer can be grown up only on a silicon substrate 11 by adjusting material gas, membrane formation temperature, etc., without growing up an epitaxial layer on the isolation insulator layer 14.
[0077] However, in order that epitaxial layers 21 and 29 may grow up to be also a longitudinal direction, finally epitaxial layers 21 and 29 are formed also on the isolation insulator layer 14.
[0078] Next, as shown in drawing 67 , with ion-implantation, in a silicon substrate 11 and an epitaxial layer 21, the ion implantation of the p mold impurity is carried out, p mold well field 12 is formed, and in a silicon substrate 11 and an epitaxial layer 29, the ion implantation of the n mold impurity is carried out, and n mold well field 13 is formed. Then, for example, silicon oxide (gate oxide) 15 and 23 is formed by the oxidizing [thermally] method on an epitaxial layer 21, 29 [12], i.e., p mold well field, and n mold well field 13.
[0079] Moreover, for example, the isolation insulator layer 14 top and silicon oxide 15, and the polish recon film 16 and 24 that contained the impurity on 23 are formed using a CVD method. Silicon oxide (cap oxide film) 17 and 25 is formed on the polish recon film 16 and 24 with a CVD method continuing. Then, PEP (photo-etching process) is performed and silicon oxide 17 and the resist film which has a predetermined pattern on 25 are formed.
[0080] This resist film is used as a mask and silicon oxide 17 and 25 is etched by RIE. Then, the resist film exfoliates. Moreover, silicon oxide 17 and 25 is used as a mask, and the polish recon film 16 and 24 is etched by RIE. Consequently, the gate electrode of MOSFET which consists of polish recon film 16 and 24 is done.
[0081] Moreover, using ion-implantation, the polish recon film (gate electrode) 16 is used as a mask, and the ion implantation of the n mold impurity is carried out into p mold well field 12 by the self aryne. Consequently, in p mold well field 12, shallow and low-concentration n mold impurity range 20, i.e., n mold extension field, is formed.
[0082] Similarly, using ion-implantation, the polish recon film (gate electrode) 24 is used as a mask, and the ion implantation of the p mold impurity is carried out into n mold well field 13 by the self aryne. Consequently, in n mold well field 13, shallow and low-concentration p mold impurity range 28, i.e., p mold extension field, is formed.
[0083] Then, it oxidizes thermally and silicon oxide is formed in the front face of the polish recon film (gate electrode) 16 and 24.
[0084] Moreover, for example, the silicon nitrides 18 and 26 which cover completely the polish recon film (gate electrode) 16 and 24 on [whole] the isolation insulator layer 14 and a component field are formed with a CVD method. Moreover, the silicon nitrides 18 and 26 are etched and these silicon nitrides 18 and 26 are made to remain only on the side attachment wall of the polish recon film 16 and 24 by RIE.
[0085] Then, using ion-implantation, the polish recon film 16 and the silicon nitride 18 are used as a mask, and the ion implantation of the n mold impurity is carried out to p mold well field 12 by the self aryne. Moreover, using ion-implantation, the polish recon film 24 and the silicon nitride 26 are used as a mask, and the ion implantation of the p

mold impurity is carried out to n mold well field 13 by the self aryne.
[0086] Consequently, in p mold well field 12, the high-concentration impurity range 19 deeper than n mold extension field 20 and, i.e., n mold source / drain field, is formed, and the high-concentration impurity range 27 deeper than p mold extension field 28 and, i.e., p mold source / drain field, is formed in n mold well field 13.
[0087] Next, as shown in drawing 68 , an interlayer insulation film 31 is formed on [whole] a silicon substrate 11 with a CVD method. Moreover, the contact hole which arrives at the contact hole, and the source / drain field 19 which reaches an interlayer insulation film 31 at the polish recon film 16, for example using PEP and an etching technique is formed.
[0088] Moreover, for example, the contact plugs 32a and 32b are formed in these contact holes using CVD and a CMP technique. Then, Wiring 33a and 33b is formed on an interlayer insulation film 31. Finally, the passivation film 34 is formed on an interlayer insulation film 31 with a CVD method.
[0089] The CMOS integrated circuit constituted from an epitaxial layer 21 and an MOSFET formed in 29 by the above process is completed.
[0090] The description of this CMOS integrated circuit is in the point that a part of source / drain field 19 are arranged on the isolation insulator layer 14 while MOSFET is formed in an epitaxial layer 21, as shown in drawing 69 . For this reason, it is possible to make small area of the junction interface of the well field 12, and the source / drain field 19, and sharp reduction of parasitic capacitance is possible.
[0091]
[Problem(s) to be Solved by the Invention] In the conventional example shown in above-mentioned (1) and (2), epitaxial layers 21 and 29 are alternatively formed on a silicon substrate 11, respectively. Here, as for epitaxial layers 21 and 29, growth advances equally from a front face to the lengthwise direction and longitudinal direction of a silicon substrate 11 at the time of selection epitaxial growth. For this reason, epitaxial layers 21 and 29 will be formed also on the isolation insulator layer 14.
[0092] In this case, as shown in drawing 70 , before forming epitaxial layers 21 and 29, after isolation width of face forms epitaxial layers 21 and 29 to being A (width of face of the isolation insulator layer 14), it is set to B (= A-2t). However, t is the thickness of epitaxial layers 21 and 29. That is, finally isolation width of face becomes narrower than the width of face of the isolation insulator layer 14.
[0093] Therefore, when the minimum isolation width of face demanded on a property, i.e., final isolation width of face, is assumed to be a and the thickness of epitaxial layers 21 and 29, i.e., the width of face to which epitaxial layers 21 and 29 enter on the isolation insulator layer 14, is assumed to be t as shown in drawing 71 for example, the width of face b of the isolation insulator layer 14 must be set as (a+2t).
[0094] Moreover, when the width of face (width of face of an epitaxial layer) of a final component field is assumed to be c, the width of face d of the component field before forming an epitaxial layer must be set as (c-2t).
[0095] However, the width of face d of the component field before forming an epitaxial layer receives effect in the minimum processing dimension h in a photolithography. That is, width of face d cannot be made narrower than this minimum processing dimension h. Therefore, on count, even when width of face d becomes narrower than the minimum processing dimension h, since width of face d is narrowed only to the minimum processing dimension h, as a result, a component field becomes large and it causes [of the degree of integration of a component] a fall in practice.
[0096] Moreover, the growth rate of an epitaxial layer changes with the class and magnitude of a substrate. For example, the growth rate of the epitaxial layer formed on p mold well field differs from the growth rate of the epitaxial layer formed on n mold well field mutually. Moreover, if the growth rate of the epitaxial layer which will be formed on a component field if a component field (exposure product of a silicon substrate) becomes small becomes slow and a component field becomes large, the growth rate of the epitaxial layer formed on a component field will become quick.
[0097] Thus, since the growth rate of an epitaxial layer changes with the classes and magnitude of a substrate, according to the part where a growth rate is in practice the slowest, it has decided on the growth time amount of an epitaxial layer. In this case, in the part where a growth rate is the quickest, isolation width of face becomes narrower than the value a of an ideal, or epitaxial layers join together in two component fields which adjoin in being the worst, and the situation which both the components field short-circuits arises.
[0098] In order to avoid such a situation, in consideration of dispersion in the growth rate of an epitaxial layer, the margin of deltab must be further set as the width of face b of the isolation insulator layer 14. However, making large further width of face of the isolation insulator layer 14 brings about the fall of the degree of integration of a component, and increase of a chip size.
[0099] Thus, in the CMOS integrated circuit which consists of MISFET which has the conventional EREBETEDDO source / drain structure, and MISFET formed in an epitaxial layer, in order that an epitaxial layer may grow up to be a

lengthwise direction and a longitudinal direction isotropic, an epitaxial layer is formed also on an isolation insulator layer.
[0100] For this reason, in consideration of dispersion in the growth rate of an epitaxial layer, it is necessary to set up the width of face of an isolation insulator layer width, and to set up the width of face of the component field in front of epitaxial growth straitness, and to set up only predetermined margin-width deltab width further about an isolation insulator layer.
[0101] Therefore, in the CMOS integrated circuit which consists of MISFET which has the conventional EREBETEDDO source / drain structure, and MISFET formed in an epitaxial layer, the degree of integration of a component fell and there was a problem of a chip size increasing.
[0102] It was made that this invention should solve the above-mentioned trouble, and the purpose is proposing the new structure improvement in the degree of integration of a component and contraction of a chip size being aimed at in the semiconductor device which consists of MISFET of the EREBETEDDO source / drain structure, MISFET formed in an epitaxial layer.
[0103]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the semiconductor device of this invention It has the 1st and 2nd MISFET(s) formed on a semi-conductor substrate, and the isolation insulator layer which separates said 1st and 2nd MISFET(s) electrically. Said 1st and 2nd MISFET(s) It has the EREBETEDDO source / drain structure arranged in the location where the front face of the source / drain field is higher than the channel formed in the front face of said semi-conductor substrate, and the stopper insulator layer which has the width of face below the width of face of said isolation insulator layer is arranged on said isolation insulator layer.
[0104] The width of face of said stopper insulator layer is substantially [as the width of face of said isolation insulator layer] the same, and the height from the front face of said semi-conductor substrate to the top face of said stopper insulator layer is more than height from the front face of said semi-conductor substrate to the front face of said source / drain field.
[0105] the width of face of said stopper insulator layer -- the width of face of said isolation insulator layer -- narrow -- height H from the front face of said semi-conductor substrate to the top face of said stopper insulator layer, and height T' from the front face of said semi-conductor substrate to the front face of said source / drain field -- H+X>=T -- ' (however, X is taken as the distance from the edge section of said isolation insulator layer to the edge section of said stopper insulator layer.) -- it has relation.
[0106] The semiconductor device of this invention is equipped with MISFET formed on a semi-conductor substrate, and the isolation insulator layer which encloses said MISFET. On said isolation insulator layer The stopper insulator layer which encloses said MISFET in the range larger than the range where said isolation insulator layer encloses said MISFET is arranged. Within limits by which said stopper insulator layer encloses said MISFET, the semi-conductor layer used as the source / drain field of said MISFET is filled, and said semi-conductor layer on said isolation insulator layer constitutes the contact field to said source / drain field.
[0107] Towards the gate electrode of said MISFET being prolonged, the width of face of the range where said stopper insulator layer encloses said MISFET is substantially equal to the width of face of the range where said isolation insulator layer encloses said MISFET, and the width of face of the range where said stopper insulator layer encloses said MISFET is larger than the width of face of the range where said isolation insulator layer encloses said MISFET towards crossing in the direction in which the gate electrode of said MISFET is prolonged.
[0108] The 1st and the 2nd element field where the semiconductor device of this invention is arranged in a semi-conductor substrate, The isolation insulator layer formed between said the 1st and 2nd element fields, and the stopper insulator layer which has width of face narrower than the width of face of said isolation insulator layer, and is arranged on said isolation insulator layer, The semi-conductor layer formed at said 1st [the] and the 2nd element field top list on said isolation insulator layer except said stopper insulator layer top, The 1st MISFET to which it is formed in said semi-conductor layer on said 1st element field, and a part of base of the source / drain field contacts said isolation insulator layer, It is formed in said semi-conductor layer on said 2nd element field, and a part of base of the source / drain field is equipped with the 2nd MISFET in contact with said isolation insulator layer.
[0109] height H from the front face of said semi-conductor substrate to the top face of said stopper insulator layer, and height T' from the front face of said semi-conductor substrate to the front face of said semi-conductor layer -- H+X>=T -- ' (however, X is taken as the distance from the edge section of said isolation insulator layer to the edge section of said stopper insulator layer.) -- it has relation.
[0110] The 1st and 2nd MISFET(s) by which the semiconductor device of this invention is formed on a semi-conductor substrate, It has the isolation insulator layer which separates said 1st and 2nd MISFET(s) electrically. Said 1st and 2nd

MISFET(s) It has the EREBETEDDO source / drain structure arranged in the location where the front face of the source / drain field is higher than the channel formed in the front face of said semi-conductor substrate. On said isolation insulator layer, while becoming the source / drain field of said 1st and 2nd MISFET(s), the semi-conductor layer which connects said 1st and 2nd MISFET(s) electrically is formed.

[0111] The 1st and the 2nd element field where the semiconductor device of this invention is arranged in a semi-conductor substrate, The isolation insulator layer formed between said the 1st and 2nd element fields, and the semi-conductor layer formed on said the 1st and 2nd element field, and said isolation insulator layer, The 1st MISFET formed in said semi-conductor layer on said 1st element field, It has the 2nd MISFET formed in said semi-conductor layer on said 2nd element field, and the source / drain field of said 1st and 2nd MISFET(s) are mutually combined in said semi-conductor layer on said isolation insulator layer.

[0112] In each above-mentioned semiconductor device, said stopper insulator layer consists of ingredients which have etch selectivity to said isolation insulator layer. Moreover, the front face of said semi-conductor substrate and the front face of said isolation insulator layer are substantially in agreement.

[0113] The 1st and 2nd MISFET(s) by which the semiconductor device of this invention is formed on a semi-conductor substrate, It has the isolation insulator layer of STI structure which separates said 1st and 2nd MISFET(s) electrically. Said 1st and 2nd MISFET(s) It has the EREBETEDDO source / drain structure arranged in the location where the front face of the source / drain field is higher than the channel formed in the front face of said semi-conductor substrate. A hollow is established in the edge section of said isolation insulator layer, and the semi-conductor layer used as the source / drain field of said 1st and 2nd MISFET(s) is filled in said hollow.

[0114] The 1st and the 2nd element field where the semiconductor device of this invention is arranged in a semi-conductor substrate, The isolation insulator layer of STI structure which is formed between said the 1st and 2nd element fields, and has a hollow in the edge section, The semi-conductor layer formed on said the 1st and 2nd element field and in the hollow of said isolation insulator layer, The 1st MISFET to which it is formed in said semi-conductor layer on said 1st element field, and a part of base of the source / drain field contacts said isolation insulator layer, It was formed in said semi-conductor layer on said 2nd element field, and a part of base of the source / drain field is equipped with the 2nd MISFET in contact with said isolation insulator layer.

[0115]

[Embodiment of the Invention] Hereafter, the semiconductor device of this invention is explained to a detail, referring to a drawing.

[0116] Drawing 1 shows the semiconductor device in connection with the gestalt of the 1st operation of this invention.

[0117] This semiconductor device is related with MOSFET which has the EREBETEDDO source / drain structure which constitutes a CMOS integrated circuit.

[0118] In the single crystal silicon substrate 11, p mold well field 12 and n mold well field 13 are formed. A silicon substrate 11 may be n mold, or may be p mold. Between p mold well field 12 and n mold well field 13, the isolation insulator layer 14 of STI structure is formed. The front face of the isolation insulator layer 14 is in agreement with the front face of a silicon substrate 11 in general.

[0119] The n channel mold MOSFET is formed on p mold well field 12.

[0120] That is, on p mold well field 12, the polish recon film (gate electrode) 16 containing silicon oxide (gate dielectric film) 15 and an impurity is formed. On the polish recon film 16, the silicon oxide (cap oxide film) 17 used as the mask at the time of processing the polish recon film 16 is formed. Moreover, the silicon nitride (side-attachment-wall insulator layer) 18 is formed in the side attachment wall of the polish recon film 16.

[0121] In p mold well field 12, low-concentration n mold extension field 20 is formed rather than n mold source / drain field 19, and this the source / drain field 19. That is, the source / drain field 19 is formed in p mold well field 12 of the both sides of the polish recon film 16, and n mold extension field 20 is formed in p mold well field [directly under] 12 of the silicon nitride 18.

[0122] On a silicon substrate 11 (the source / drain field 19), an epitaxial layer 21 is formed alternatively. Since an epitaxial layer 21 consists of single crystal silicon and contains the impurity of n mold like the silicon substrate 11 (the source / drain field 19), it has become a part of source / drain field 19.

[0123] On an epitaxial layer (the source / drain field) 21, the refractory metal silicide layers (a tungsten silicide layer, titanium silicide layer, etc.) 22 are formed. In this example, although the refractory metal silicide layer 22 is not formed on the polish recon film (gate electrode) 16, it may remove silicon oxide (cap oxide film) 17, and may form it on the polish recon film 16.

[0124] The p channel mold MOSFET is formed on n mold well field 13.

[0125] That is, on n mold well field 13, the polish recon film (gate electrode) 24 containing silicon oxide (gate

dielectric film) 23 and an impurity is formed. On the polish recon film 24, the silicon oxide (cap oxide film) 25 used as the mask at the time of processing the polish recon film 24 is formed. Moreover, the silicon nitride (side-attachment-wall insulator layer) 26 is formed in the side attachment wall of the polish recon film 24.

[0126] In n mold well field 13, low-concentration p mold extension field 28 is formed rather than p mold source / drain field 27, and this the source / drain field 27. That is, the source / drain field 27 is formed in n mold well field 13 of the both sides of the polish recon film 24, and p mold extension field 28 is formed in n mold well field [directly under] 13 of the silicon nitride 26.

[0127] On a silicon substrate 11 (the source / drain field 27), an epitaxial layer 29 is formed alternatively. Since an epitaxial layer 29 consists of single crystal silicon and contains the impurity of p mold like the silicon substrate 11 (the source / drain field 27), it has become a part of source / drain field 27.

[0128] On an epitaxial layer (the source / drain field) 29, the refractory metal silicide layers (a tungsten silicide layer, titanium silicide layer, etc.) 30 are formed. In this example, although the refractory metal silicide layer 30 is not formed on the polish recon film (gate electrode) 24, it may remove silicon oxide (cap oxide film) 25, and may form it on the polish recon film 24.

[0129] The stopper insulator layer 35 is formed on the isolation insulator layer 14. The stopper insulator layer 35 has the same size as the isolation insulator layer 14, and the same pattern, when it sees from a silicon substrate 11.

[0130] Moreover, the stopper insulator layer 35 makes growth of the longitudinal direction of the epitaxial layers 21 and 29 at the time of selection epitaxial growth stop. Therefore, the height from the front face of a silicon substrate 11 to the top face of the stopper insulator layer 35 is the same as the height from the front face of a silicon substrate 11 to the top face of the refractory metal silicide layers 22 and 30, or higher than it.

[0131] According to the semiconductor device of the above-mentioned configuration, since the stopper insulator layer 35 is arranged on the isolation insulator layer 14, an epitaxial layer 21 and an epitaxial layer 29 do not contact mutually on the component isolation region 14. Moreover, if the width of face of the stopper insulator layer 35 is set as the minimum isolation width of face a of which it is required on a property in order that an epitaxial layer 21 and an epitaxial layer 29 may leave mutually only the width of face of the stopper insulator layer 35, an isolation property will not get worse.

[0132] Next, the manufacture approach of the semiconductor device of the gestalt the 1st above-mentioned operation is explained.

[0133] First, as shown in drawing 2 , the isolation insulator layer 14 of STI structure is formed in the single crystal silicon substrate 11. Moreover, p mold well field 12 and n mold well field 13 are formed in a silicon substrate 11, and silicon oxide (gate oxide) 15 and 23 is formed on the component field enclosed by the isolation insulator layer 14.

[0134] Moreover, as usual, on p mold well field 12, the polish recon film (gate electrode) 16, silicon oxide (cap oxide film) 17, and the silicon nitride (side-attachment-wall insulator layer) 18 are formed, and shallow and low-concentration n mold impurity range 20, i.e., n mold extension field, is formed in p mold well field 12.

[0135] Moreover, on n mold well field 13, the polish recon film (gate electrode) 24, silicon oxide (cap oxide film) 25, and the silicon nitride (side-attachment-wall insulator layer) 26 are formed, and shallow and low-concentration p mold impurity range 28, i.e., p mold extension field, is formed in n mold well field 13.

[0136] Then, for example, the stopper insulator layer 35 is formed on [whole] a silicon substrate 11 with a CVD method. Although the stopper insulator layer 35 may be constituted from what kind of thing as long as it is an ingredient which has insulation, a silicon nitride, its silicon oxide, etc. are realistic, for example.

[0137] Moreover, PEP (photo-etching process) is performed and the same pattern as the isolation insulator layer 14 and the resist film 36 of the same size are formed on the stopper insulator layer 35 on the isolation insulator layer 14. In forming the resist film 36, the pattern of the mask (reticle) used, for example in order to form the trench for STI in a silicon substrate 11 can be used.

[0138] This resist film 36 is used as a mask, by RIE, the stopper insulator layer 35 is etched and the same pattern as the isolation insulator layer 14 and the stopper insulator layer 35 of the same size are formed on the isolation insulator layer 14. Then, the resist film 36 exfoliates.

[0139] In addition, in this example, the width of face of the isolation insulator layer 14 and the width of face of the stopper insulator layer 35 are the minimum isolation width of face a demanded on a property, respectively.

[0140] Next, as shown in drawing 3 , the silicon oxide 15 and 23 which exists in the both sides of the polish recon film 16 and 24 is removed, and a silicon substrate 11 20, i.e., n mold extension field, and p mold extension field 28 are exposed.

[0141] Next, as shown in drawing 4 , while forming alternatively an epitaxial layer (single-crystal-silicon layer) 21 with selection epitaxial growth on n mold extension field 20 (silicon substrate 11) which became unreserved, an

epitaxial layer (single-crystal-silicon layer) 29 is alternatively formed on p mold extension field 28 (silicon substrate 11) which became unreserved.
[0142] In this example, since silicon oxide 17 and 25 exists on the polish recon film 16 and 24, an epitaxial layer does not grow on the polish recon film 16 and 24. However, in removing silicon oxide 17 and 25 beforehand, on the polish recon film 16 and 24, a polish recon epitaxial layer grows at the time of selection epitaxial growth.
[0143] Moreover, when the height t1 from the front face of a silicon substrate 11 to the top face of the stopper insulator layer 35, i.e., the front face of the isolation insulator layer 14 and the front face of a silicon substrate 11, is substantially equal, the height (thickness) t2 of epitaxial layers 21 and 29 is the same as the height of the stopper insulator layer 35, or it is adjusted so that it may become lower than it.
[0144] In two components (MOSFET) which adjoin mutually by this, the minimum isolation width of face a demanded on a property is secured.
[0145] Next, as shown in drawing 5 , using ion-implantation, the polish recon film 16 and the silicon nitride 18 are used as a mask, and the ion implantation of the n mold impurity is carried out into p mold well field 12 and an epitaxial layer 21 by the self aryne. Moreover, using ion-implantation, the polish recon film 24 and the silicon nitride 26 are used as a mask, and the ion implantation of the p mold impurity is carried out into n mold well field 13 and an epitaxial layer 29 by the self aryne.
[0146] Consequently, in p mold well field 12 and an epitaxial layer 21, the high-concentration impurity range 19 deeper than n mold extension field 20 and, i.e., n mold source / drain field, is formed, and the high-concentration impurity range 27 deeper than p mold extension field 28 and, i.e., p mold source / drain field, is formed in n mold well field 13 and an epitaxial layer 29.
[0147] Moreover, for example, refractory metal film (a tungsten, titanium, etc.) is formed with a CVD method on an epitaxial layer 21 and the whole surface of the silicon substrate 11 including 29 tops. Then, if annealing is performed (like a heat process), an epitaxial layer 21, and the silicon and the refractory metal film in 29 will react chemically, and the refractory metal silicide layers 22 and 30 will be formed in the upper part of epitaxial layers 21 and 29.
[0148] Then, the unreacted refractory metal film is removed.
[0149] Here, when removing beforehand the polish recon film (gate electrode) 16 and the silicon oxide 17 and 25 on 24, at the time of annealing, the polish recon film 16 and 24 and the refractory metal film react chemically, and a refractory metal silicide layer is formed also in the upper part of the polish recon film 16 and 24.
[0150] MOSFET which has the EREBETEDDO source / drain structure which constitutes a CMOS integrated circuit according to the above process is completed.
[0151] Drawing 6 shows the semiconductor device in connection with the gestalt of the 2nd operation of this invention.

[0152] This semiconductor device is related with MOSFET which has the EREBETEDDO source / drain structure which constitutes a CMOS integrated circuit.
[0153] As compared with the semiconductor device in connection with the gestalt of the 1st above-mentioned operation in the semiconductor device in connection with the gestalt of this operation, the stopper insulator layer 35 on the isolation insulator layer 14 differs from the configuration of epitaxial layers 21 and 29. That is, about other points, it is the same as the semiconductor device of the gestalt of the 1st above-mentioned operation.
[0154] Hereafter, a part which is different from the semiconductor device in connection with the gestalt of the 1st above-mentioned operation about the semiconductor device of the gestalt of this operation, and the part relevant to this are explained.
[0155] The stopper insulator layer 35 is formed on the isolation insulator layer 14. The width of face of the stopper insulator layer 35 is narrower than the width of face of the isolation insulator layer 14, when it sees from a silicon substrate 11. That is, the width of face of the stopper insulator layer 35 is the minimum isolation width of face a demanded on a property, and the width of face of the isolation insulator layer 14 is larger than the minimum isolation width of face a demanded on a property.
[0156] Moreover, the height from the front face of a silicon substrate 11 to the top face of the stopper insulator layer 35 is the same as the height from the front face of a silicon substrate 11 to the top face of the refractory metal silicide layers 22 and 30, or higher than it. Therefore, the stopper insulator layer 35 makes growth of the longitudinal direction of the epitaxial layers 21 and 29 at the time of selection epitaxial growth stop.
[0157] Epitaxial layers (the source / drain field) 21 and 29 are formed also on the isolation insulator layer 14. That is, since the contact field to the source / drain field is prepared on an epitaxial layer 21 and 29, it can make small the plane-of-composition product of the source / drain fields 19 and 27, and the well fields 12 and 13 regardless of a contact field.

[0158] In the semiconductor device of the above-mentioned configuration, since the stopper insulator layer 35 is arranged on the isolation insulator layer 14, an epitaxial layer 21 and an epitaxial layer 29 do not contact mutually on the component isolation region 14. Moreover, if the width of face of the stopper insulator layer 35 is set as the minimum isolation width of face a of which it is required on a property in order that an epitaxial layer 21 and an epitaxial layer 29 may leave mutually only the width of face of the stopper insulator layer 35, an isolation property will not get worse.
[0159] Next, the manufacture approach of the semiconductor device of the gestalt the 2nd above-mentioned operation is explained.
[0160] First, as shown in drawing 7 , the isolation insulator layer 14 of STI structure is formed in the single crystal silicon substrate 11. Moreover, p mold well field 12 and n mold well field 13 are formed in a silicon substrate 11, and silicon oxide (gate oxide) 15 and 23 is formed on the component field enclosed by the isolation insulator layer 14.
[0161] Moreover, as usual, on p mold well field 12, the polish recon film (gate electrode) 16, silicon oxide (cap oxide film) 17, and the silicon nitride (side-attachment-wall insulator layer) 18 are formed, and shallow and low-concentration n mold impurity range 20, i.e., n mold extension field, is formed in p mold well field 12.
[0162] Moreover, on n mold well field 13, the polish recon film (gate electrode) 24, silicon oxide (cap oxide film) 25, and the silicon nitride (side-attachment-wall insulator layer) 26 are formed, and shallow and low-concentration p mold impurity range 28, i.e., p mold extension field, is formed in n mold well field 13.
[0163] Then, for example, the stopper insulator layer 35 is formed on [whole] a silicon substrate 11 with a CVD method. Although the stopper insulator layer 35 may be constituted from what kind of thing as long as it is an ingredient which has insulation, a silicon nitride, its silicon oxide, etc. are realistic, for example.
[0164] Moreover, PEP (photo-etching process) is performed and the resist film 36 which has the width of face a narrower than the width of face W of the isolation insulator layer 14 is formed on the stopper insulator layer 35 on the isolation insulator layer 14. This resist film 36 is used as a mask, by RIE, the stopper insulator layer 35 is etched and the stopper insulator layer 35 which has width of face narrower than the width of face W of the isolation insulator layer 14 on the isolation insulator layer 14 is formed. Then, the resist film 36 exfoliates.
[0165] In addition, in this example, the width of face of the stopper insulator layer 35 is the minimum isolation width of face a demanded on a property.
[0166] Next, as shown in drawing 8 , the silicon oxide 15 and 23 which exists in the both sides of the polish recon film 16 and 24 is removed, and a silicon substrate 11 20, i.e., n mold extension field, and p mold extension field 28 are exposed.
[0167] Next, as shown in drawing 9 , while forming alternatively an epitaxial layer (single-crystal-silicon layer) 21 with selection epitaxial growth on n mold extension field 20 (silicon substrate 11) which became unreserved, an epitaxial layer (single-crystal-silicon layer) 29 is alternatively formed on p mold extension field 28 (silicon substrate 11) which became unreserved.
[0168] At the time of selection epitaxial growth, be [epitaxial layers 21 and 29 / isotropic], i.e., in order to grow up to be a lengthwise direction and a longitudinal direction, epitaxial layers 21 and 29 will be formed also on the isolation insulator layer 14.
[0169] However, the stopper insulator layer 35 exists among epitaxial layers 21 and 29. Therefore, about two components (MOSFET) which adjoin mutually, the minimum isolation width of face a demanded on a property is secured.
[0170] Next, as shown in drawing 10 , using ion-implantation, the polish recon film 16 and the silicon nitride 18 are used as a mask, and the ion implantation of the n mold impurity is carried out into p mold well field 12 and an epitaxial layer 21 by the self aryne. Moreover, using ion-implantation, the polish recon film 24 and the silicon nitride 26 are used as a mask, and the ion implantation of the p mold impurity is carried out into n mold well field 13 and an epitaxial layer 29 by the self aryne.
[0171] Consequently, in p mold well field 12 and an epitaxial layer 21, the high-concentration impurity range 19 deeper than n mold extension field 20 and, i.e., n mold source / drain field, is formed, and the high-concentration impurity range 27 deeper than p mold extension field 28 and, i.e., p mold source / drain field, is formed in n mold well field 13 and an epitaxial layer 29.
[0172] Moreover, for example, refractory metal film (a tungsten, titanium, etc.) is formed with a CVD method on an epitaxial layer 21 and the whole surface of the silicon substrate 11 including 29 tops. Then, if annealing is performed (like a heat process), an epitaxial layer 21, and the silicon and the refractory metal film in 29 will react chemically, and the refractory metal silicide layers 22 and 30 will be formed in the upper part of epitaxial layers 21 and 29.
[0173] Then, the unreacted refractory metal film is removed.

[0174] In addition, the polish recon film (gate electrode) 16 and the silicon oxide 17 and 25 on 24 are removed beforehand, and a refractory metal silicide layer may be formed in the upper part of the polish recon film 16 and 24 at the time of annealing.
[0175] MOSFET which has the EREBETEDDO source / drain structure which constitutes a CMOS integrated circuit according to the above process is completed.
[0176] Next, in the semiconductor device in the gestalt of the 2nd above-mentioned operation, the relation of the height of the stopper insulator layer which makes growth of the longitudinal direction of epitaxial layer thickness and an epitaxial layer stop is considered.
[0177] First, the width of face of the stopper insulator layer 35 is narrower than the width of face of the isolation insulator layer 14, and width of face from the edge section (boundary of a silicon substrate 11 and the isolation insulator layer 14) of the isolation insulator layer 14 to the edge section of the stopper insulator layer 35 is set to X.
[0178] Moreover, the height from the front face of a silicon substrate 11 to the top face of the stopper insulator layer 35 is set to H. In this example, the front face of a silicon substrate 11 and the top face of the isolation insulator layer 14 are assumed to be what is mutually in agreement. Therefore, height H from the front face of a silicon substrate 11 to the top face of the stopper insulator layer 35 becomes the height of the stopper insulator layer 35.
[0179] Under such conditions, thickness T of an epitaxial layer 21 examines as max and which grade it can be set.
[0180] The point in the longitudinal direction of an epitaxial layer 21 is observed.
[0181] First, if epitaxial growth shall advance isotropic as shown in drawing 11 and drawing 12 , the point in the longitudinal direction of an epitaxial layer 21 will reach the root (edge at the bottom) of the stopper insulator layer 35, when the stopper insulator layer 35 is approached and the thickness of an epitaxial layer 21 was set to X as the thickness of an epitaxial layer 21 increased.
[0182] If the point of an epitaxial layer 21 reaches the root of the stopper insulator layer 35, from here, an epitaxial layer 21 cannot grow up to be a longitudinal direction. Therefore, the point of an epitaxial layer 21 grows up to be a lengthwise direction in accordance with the side attachment wall of the stopper insulator layer 35.
[0183] When thickness T of an epitaxial layer 21 becomes T' (>X) as shown in drawing 13 since growth of an epitaxial layer 21 is isotropic, as for the tip of an epitaxial layer 21, only (T'-X) is creeping up from the root of the stopper insulator layer 35.
[0184] Therefore, in order for an epitaxial layer 21 not to overcome the stopper insulator layer 35, <=(T'-X) H, i.e., thickness T of an epitaxial layer 21, is T = T'<= (H+X). -- (1)
It is necessary to fulfill the becoming conditions.
[0185] In addition, since it is X= 0 with the gestalt of the 1st above-mentioned operation, it is T= from the above-mentioned (1) formula. T'<= It is set to H. That is, the height of the stopper insulator layer 35 is the same as the thickness of an epitaxial layer 21, or higher than it.
[0186] Next, the membrane formation rate of the epitaxial layer in selection epitaxial growth is examined.
[0187] The membrane formation rate of an epitaxial layer changes with classes, magnitude, etc. of a substrate, as explained also in the Prior art. It is coped with by generally forming an epitaxial layer to dispersion in such a membrane formation rate on conditions from which sufficient thickness is obtained in the latest part of a membrane formation rate.

[0188] Here, growth of an epitaxial layer makes Er' the membrane formation rate in the latest part, and makes Er" the membrane formation rate in the part where growth of an epitaxial layer is the quickest. Moreover, the epitaxial layer thickness in the part where growth of te and an epitaxial layer is the slowest will be set for it in the part where growth of an epitaxial layer is the slowest, if membrane formation time amount is set to Tm (set point), and it is Er'xte. = Tm -- (2)
What is necessary will be just to become.
[0189] Setting on the other hand in the part where growth of an epitaxial layer is the quickest, epitaxial layer thickness is T". = Er"xte= (Er"/Er') xTm -- (3)
It becomes.
[0190] That is, epitaxial layer thickness T" in the part where growth of an epitaxial layer is the quickest than the above-mentioned (1) formula is T = T"<= (H+X). -- (4)
What is necessary will be just to ******.
[0191] Therefore, the above (3) and (4) types (Er"/Er') xTm <= (H+X) -- (5)
The becoming conditions are drawn.
[0192] In addition, it is Er"=Er'=Er, when it is not based on a class, magnitude, etc. of a substrate but the membrane formation rate of epitaxial growth assumes on a wafer that it is always fixed. Since it becomes Tm=Erxte, it is the

above-mentioned (5) formula. Tm = Erxte <= (H+X) -- (6)
It becomes.
[0193] Drawing 14 and drawing 15 show the semiconductor device in connection with the gestalt of the 3rd operation of this invention. Drawing 15 is a sectional view which meets the XV-XV line of drawing 14 R> 4.
[0194] This semiconductor device is related with MOSFET which has the EREBETEDDO source / drain structure. Although the following explanation is given about the n channel mold MOSFET, naturally it is applicable also about the p channel mold MOSFET.
[0195] In the single crystal silicon substrate 11, the isolation insulator layer 14 of STI structure is formed. p mold well field 12 is formed in the component field (surface section of a silicon substrate 11) enclosed by the isolation insulator layer 14. A silicon substrate 11 may be n mold, or may be p mold.
[0196] The front face of a silicon substrate 11 and the front face of the isolation insulator layer 14 are in agreement in general. If the front face of the isolation insulator layer 14 is made in agreement with the front face of a silicon substrate 11 in general, it will be because processing of the gate electrode formed ranging over a silicon substrate 11 and the isolation insulator layer 14 can carry out easily for example.
[0197] The n channel mold MOSFET is formed on p mold well field 12.
[0198] That is, on p mold well field 12, the polish recon film (gate electrode) 16 containing silicon oxide (gate dielectric film) 15 and an impurity is formed. On the polish recon film 16, the silicon oxide (cap oxide film) 17 used as the mask at the time of processing the polish recon film 16 is formed. Moreover, the silicon nitride (side-attachment-wall insulator layer) 18 is formed in the side attachment wall of the polish recon film 16.
[0199] The polish recon film (gate electrode) 16 had the Rhine pattern, for example, is prolonged on the isolation insulator layer 14 from on the component field (p mold well field). Moreover, the polish recon film 16 has the contact field 37 on the isolation insulator layer 14.
[0200] In p mold well field 12, low-concentration n mold extension field 20 is formed rather than n mold source / drain field 19, and this the source / drain field 19. That is, the source / drain field 19 is formed in p mold well field 12 of the both sides of the polish recon film 16, and n mold extension field 20 is formed in p mold well field [directly under] 12 of the silicon nitride 18.
[0201] On a silicon substrate 11 (the source / drain field 19), an epitaxial layer 21 is formed alternatively. An epitaxial layer 21 is formed also on the isolation insulator layer 14 while it is formed on the source / drain field 19. Since an epitaxial layer 21 consists of single crystal silicon and contains the impurity of n mold like the silicon substrate 11 (the source / drain field 19), it has become a part of source / drain field 19.
[0202] The stopper insulator layer 35 is formed on the isolation insulator layer 14. The stopper insulator layer 35 is arranged so that a component field may be surrounded. However, the area size which the stopper insulator layer 35 encloses is somewhat larger than a component field. For example, in the direction in which the polish recon film (gate electrode) 16 is prolonged, the width of face of a field and the width of face of a component field which the stopper insulator layer 35 encloses are equal. Moreover, in the direction perpendicular to the direction in which the polish recon film 16 is prolonged, the width of face of the field which the stopper insulator layer 35 encloses is larger than the width of face of a component field.
[0203] It will be filled by the epitaxial layer 21 in the field which the stopper insulator layer 35 encloses. That is, an epitaxial layer 21 is not formed in the exterior of the field which the stopper insulator layer 35 encloses.
[0204] On an epitaxial layer (the source / drain field) 21, the refractory metal silicide layers (a tungsten silicide layer, titanium silicide layer, etc.) 22 are formed. In this example, although the refractory metal silicide layer 22 is not formed on the polish recon film (gate electrode) 16, it may remove silicon oxide (cap oxide film) 17, and may form it on the polish recon film 16.
[0205] The contact field 38 to an epitaxial layer (the source / drain field) 21 is established in the epitaxial layer 21 on the isolation insulator layer 14. Thereby, regardless of the magnitude of the contact field 38, the plane-of-composition product of p mold well field 12, and the n mold source / drain field 19 can be reduced.
[0206] Next, the manufacture approach of the semiconductor device of the gestalt the 3rd above-mentioned operation is explained.
[0207] First, as shown in drawing 16 and drawing 17 , the isolation insulator layer 14 of STI structure is formed in the single crystal silicon substrate 11.
[0208] Next, as shown in drawing 18 and drawing 19 , with ion-implantation, in a silicon substrate 11, the ion implantation of the p mold impurity is carried out, and p mold well field 12 is formed. Then, for example, silicon oxide (gate oxide) 15 is formed on the component field enclosed by the isolation insulator layer 14 by the oxidizing [thermally] method.

[0209] Moreover, for example, the polish recon film 16 containing an impurity is formed on the isolation insulator layer 14 and silicon oxide 15 using a CVD method. Silicon oxide (cap oxide film) 17 is formed on the polish recon film 16 with a CVD method continuing. Then, patterning of the silicon oxide 17 is carried out, further, this silicon oxide 17 is used as a mask, by RIE, the polish recon film 16 is etched and the gate electrode of MOSFET is formed.
[0210] Moreover, using ion-implantation, the polish recon film (gate electrode) 16 is used as a mask, and the ion implantation of the n mold impurity is carried out into p mold well field 12 by the self aryne. Consequently, in p mold well field 12, shallow and low-concentration n mold impurity range 20, i.e., n mold extension field, is formed.
[0211] Then, it oxidizes thermally and silicon oxide is formed in the front face of the polish recon film (gate electrode) 16.
[0212] Moreover, for example, the silicon nitride 18 which covers the polish recon film (gate electrode) 16 completely on [whole] the isolation insulator layer 14 and a component field is formed with a CVD method. Moreover, the silicon nitride 18 is etched and this silicon nitride 18 is made to remain only on the side attachment wall of the polish recon film 16 by RIE.
[0213] Then, for example, the stopper insulator layer 35 is formed on [whole] a silicon substrate 11 with a CVD method. Although the stopper insulator layer 35 may be constituted from what kind of thing as long as it is an ingredient which has insulation, a silicon nitride, its silicon oxide, etc. are realistic, for example.
[0214] Moreover, PEP (photo-etching process) is performed and the resist film which has the pattern which encloses a component field is formed on the stopper insulator layer 35 on the isolation insulator layer 14. This resist film is used as a mask, by RIE, the stopper insulator layer 35 is etched and the stopper insulator layer 35 which encloses a component field on the isolation insulator layer 14 is formed. Then, the resist film exfoliates.
[0215] In addition, the field which the stopper insulator layer 35 encloses is somewhat larger than a component field, and the width of face to the edge of the stopper insulator layer 35 serves as X from the edge (a component field and boundary of the isolation insulator layer 14) of a component field in the direction perpendicular to the direction in which the polish recon film 16 is prolonged.
[0216] Moreover, the silicon oxide 15 which exists in the both sides of the polish recon film 16 is removed, and a silicon substrate 11 20, i.e., n mold extension field, is exposed.
[0217] Next, as shown in drawing 20 and drawing 21 , an epitaxial layer (single-crystal-silicon layer) 21 is alternatively formed with selection epitaxial growth on n mold extension field 20 (silicon substrate 11) which became unreserved.
[0218] At this time, an epitaxial layer does not grow on the polish recon film 16. However, silicon oxide 17 is removed beforehand and a polish recon epitaxial layer may be grown up on the polish recon film 16 at the time of selection epitaxial growth.
[0219] Moreover, in selection epitaxial growth, an epitaxial layer 21 grows up to be isotropic, i.e., a longitudinal direction. For this reason, an epitaxial layer 21 is formed also on the isolation insulator layer 14. However, the component field is enclosed by the stopper insulator layer 35. Therefore, although an epitaxial layer 21 is filled in the field enclosed by the stopper insulator layer 35, it is not formed in the exterior of the field enclosed by the stopper insulator layer 35.
[0220] Then, using ion-implantation, the polish recon film 16 and the silicon nitride 18 are used as a mask, and the ion implantation of the n mold impurity is carried out into p mold well field 12 and an epitaxial layer 21 by the self aryne. Consequently, in p mold well field 12 and an epitaxial layer 21, the high-concentration impurity range 19 deeper than the extension field 20 and, i.e., n mold source / drain field, is formed.
[0221] Moreover, for example, refractory metal film (a tungsten, titanium, etc.) is formed with a CVD method on the whole surface of the silicon substrate 11 including an epitaxial layer 21 top. Then, if annealing is performed (like a heat process), the silicon and the refractory metal film in an epitaxial layer 21 will react chemically, and the refractory metal silicide layer 22 will be formed in the upper part of an epitaxial layer 21.
[0222] Then, the unreacted refractory metal film is removed.
[0223] According to the above process, MOSFET which has the EREBETEDDO source / drain structure is completed.
[0224] Drawing 22 thru/or drawing 24 show the semiconductor device in connection with the gestalt of the 4th operation of this invention. The sectional view where drawing 23 meets the XXIII-XXIII line of drawing 22 R> 2, and drawing 24 are sectional views which meet the XXIV-XXIV line of drawing 22 .
[0225] This semiconductor device is related with MOSFET which has the EREBETEDDO source / drain structure.
[0226] In the single crystal silicon substrate 11, the isolation insulator layer 14 of STI structure is formed. p mold well field 12 and n mold well field 13 are formed in the component field (surface section of a silicon substrate 11) enclosed by the isolation insulator layer 14. A silicon substrate 11 may be n mold, or may be p mold. The front face of the isolation insulator layer 14 is in agreement with the front face of a silicon substrate 11 in general.

[0227] The n channel mold MOSFET is formed on p mold well field 12.
[0228] That is, on p mold well field 12, the polish recon film (gate electrode) 16 containing silicon oxide (gate dielectric film) 15 and an impurity is formed. On the polish recon film 16, the silicon oxide (cap oxide film) 17 used as the mask at the time of processing the polish recon film 16 is formed. Moreover, the silicon nitride (side-attachment-wall insulator layer) 18 is formed in the side attachment wall of the polish recon film 16.
[0229] The polish recon film (gate electrode) 16 had the Rhine pattern, for example, is prolonged on the isolation insulator layer 14 from on the component field (p mold well field). Moreover, the polish recon film 16 has the contact field 37 on the isolation insulator layer 14.
[0230] In p mold well field 12, low-concentration n mold extension field 20 is formed rather than n mold source / drain field 19, and this the source / drain field 19. That is, the source / drain field 19 is formed in p mold well field 12 of the both sides of the polish recon film 16, and n mold extension field 20 is formed in p mold well field [directly under] 12 of the silicon nitride 18.
[0231] On a silicon substrate 11 (the source / drain field 19), an epitaxial layer 21 is formed alternatively. An epitaxial layer 21 is formed also on the isolation insulator layer 14 while it is formed on the source / drain field 19. The epitaxial layer 21 on the isolation insulator layer 14 constitutes the contact field 38 to the source / drain field.
[0232] Since an epitaxial layer 21 consists of single crystal silicon and contains the impurity of n mold like the silicon substrate 11 (the source / drain field 19), it has become a part of source / drain field 19.
[0233] The p channel mold MOSFET is formed on n mold well field 13.
[0234] That is, on n mold well field 13, the polish recon film (gate electrode) 24 containing silicon oxide (gate dielectric film) 23 and an impurity is formed. On the polish recon film 24, the silicon oxide (cap oxide film) 25 used as the mask at the time of processing the polish recon film 24 is formed. Moreover, the silicon nitride (side-attachment-wall insulator layer) 26 is formed in the side attachment wall of the polish recon film 24.
[0235] The polish recon film (gate electrode) 24 had the Rhine pattern, for example, is prolonged on the isolation insulator layer 14 from on the component field (n mold well field). Moreover, the polish recon film 24 has the contact field 37 on the isolation insulator layer 14.
[0236] In n mold well field 13, low-concentration p mold extension field 28 is formed rather than p mold source / drain field 27, and this the source / drain field 27. That is, the source / drain field 27 is formed in n mold well field 13 of the both sides of the polish recon film 24, and p mold extension field 28 is formed in n mold well field [directly under] 13 of the silicon nitride 26.
[0237] On a silicon substrate 11 (the source / drain field 27), an epitaxial layer 29 is formed alternatively. An epitaxial layer 29 is formed also on the isolation insulator layer 14 while it is formed on the source / drain field 27. The epitaxial layer 29 on the isolation insulator layer 14 constitutes the contact field 38 to the source / drain field.
[0238] Since an epitaxial layer 29 consists of single crystal silicon and contains the impurity of p mold like the silicon substrate 11 (the source / drain field 27), it has become a part of source / drain field 27.
[0239] The stopper insulator layer 35 is formed on the isolation insulator layer 14. The stopper insulator layer 35 is arranged so that a component field may be surrounded. Moreover, in the field which the stopper insulator layer 35 encloses, the contact field 38 to the source / drain field is also included. For example, in a direction perpendicular to the direction in which the polish recon film 16 is prolonged, the contact field 38 to the source / drain field is formed on the isolation insulator layer 14.
[0240] It will be filled by epitaxial layers 21 and 29 in the field which the stopper insulator layer 35 encloses. That is, epitaxial layers 21 and 29 are not formed in the exterior of the field which the stopper insulator layer 35 encloses.
[0241] In this example, the contact field 38 was shifted by turns and arranged so that the contact field 38 of MOSFET which adjoins mutually may not lap. Moreover, the minimum isolation width of face a demanded on a property is completely secured about MOSFET which adjoins mutually.
[0242] On an epitaxial layer (the source / drain field) 21 and 29, the refractory metal silicide layers (a tungsten silicide layer, titanium silicide layer, etc.) 22 and 30 are formed. In this example, although the refractory metal silicide layers 22 and 30 are not formed on the polish recon film (gate electrode) 16 and 24, if silicon oxide (cap oxide film) 17 and 25 is removed beforehand, a silicide layer will be formed also on the polish recon film 16 and 24.
[0243] The contact field 38 to epitaxial layers (the source / drain field) 21 and 29 is established in the epitaxial layers 21 and 29 on the isolation insulator layer 14. Thereby, regardless of the magnitude of the contact field 38, the plane-of-composition product of the well fields 12 and 13, and the source / drain fields 19 and 27 can be reduced.
[0244] Next, the manufacture approach of the semiconductor device of the gestalt the 4th above-mentioned operation is explained.
[0245] First, as shown in drawing 25 and drawing 26 , the isolation insulator layer 14 of STI structure is formed in the

single crystal silicon substrate 11.
[0246] Next, as shown in drawing 27 thru/or drawing 29 , with ion-implantation, in a silicon substrate 11, the ion implantation of the p mold impurity is carried out, p mold well field 12 is formed, and in a silicon substrate 11, the ion implantation of the n mold impurity is carried out, and n mold well field 13 is formed. Then, for example, silicon oxide (gate oxide) 15 and 23 is formed on the component field enclosed by the isolation insulator layer 14 by the oxidizing [thermally] method.
[0247] Moreover, for example, the isolation insulator layer 14 top and silicon oxide 15, and the polish recon film 16 and 24 that contained the impurity on 23 are formed using a CVD method. Silicon oxide (cap oxide film) 17 and 25 is formed on the polish recon film 16 and 24 with a CVD method continuing. Then, patterning of the silicon oxide 17 and 25 is carried out, further, these silicon oxide 17 and 25 is used as a mask, by RIE, the polish recon film 16 and 24 is etched and the gate electrode of MOSFET is formed.
[0248] Moreover, using ion-implantation, the polish recon film (gate electrode) 16 is used as a mask, and the ion implantation of the n mold impurity is carried out into p mold well field 12 by the self aryne. Similarly, using ion-implantation, the polish recon film (gate electrode) 24 is used as a mask, and the ion implantation of the p mold impurity is carried out into n mold well field 13 by the self aryne.
[0249] Consequently, in p mold well field 12, shallow and low-concentration n mold impurity range 20, i.e., n mold extension field, is formed, and shallow and low-concentration p mold impurity range 28, i.e., p mold extension field, is formed in n mold well field 13.
[0250] Then, it oxidizes thermally and silicon oxide is formed in the front face of the polish recon film (gate electrode) 16 and 24.
[0251] Moreover, for example, the silicon nitrides 18 and 26 which cover completely the polish recon film (gate electrode) 16 and 24 on [whole] the isolation insulator layer 14 and a component field are formed with a CVD method. Moreover, the silicon nitrides 18 and 26 are etched and these silicon nitrides 18 and 26 are made to remain only on the side attachment wall of the polish recon film 16 and 24 by RIE.
[0252] Then, for example, the stopper insulator layer 35 is formed on [whole] a silicon substrate 11 with a CVD method. Although the stopper insulator layer 35 may be constituted from what kind of thing as long as it is an ingredient which has insulation, a silicon nitride, its silicon oxide, etc. are realistic, for example.
[0253] Moreover, PEP (photo-etching process) is performed and the resist film which has the pattern which encloses a component field is formed on the stopper insulator layer 35 on the isolation insulator layer 14. This resist film is used as a mask, by RIE, the stopper insulator layer 35 is etched and the stopper insulator layer 35 which encloses a component field on the isolation insulator layer 14 is formed. Then, the resist film exfoliates.
[0254] In addition, in the field which the stopper insulator layer 35 encloses, the contact field on the isolation insulator layer 14 is also included.
[0255] Moreover, the silicon oxide 15 and 23 which exists in the both sides of the polish recon film 16 and 24 is removed, and a silicon substrate 11 20, i.e., n mold extension field, and p mold extension field 28 are exposed.
[0256] Next, as shown in drawing 30 thru/or drawing 32 , an epitaxial layer (single-crystal-silicon layer) 21 is alternatively formed with selection epitaxial growth on n mold extension field 20 (silicon substrate 11) which became unreserved, and an epitaxial layer (single-crystal-silicon layer) 29 is alternatively formed on p mold extension field 28 (silicon substrate 11) which became unreserved.
[0257] In selection epitaxial growth, epitaxial layers 21 and 29 grow up to be isotropic, i.e., a longitudinal direction. For this reason, epitaxial layers 21 and 29 are formed also on the isolation insulator layer 14. However, the component field is enclosed by the stopper insulator layer 35. Therefore, although epitaxial layers 21 and 29 are filled in the field enclosed by the stopper insulator layer 35, they are not formed in the exterior of the field enclosed by the stopper insulator layer 35.
[0258] Then, using ion-implantation, the polish recon film 16 and the silicon nitride 18 are used as a mask, and the ion implantation of the n mold impurity is carried out into p mold well field 12 and an epitaxial layer 21 by the self aryne. Similarly, using ion-implantation, the polish recon film 24 and the silicon nitride 26 are used as a mask, and the ion implantation of the p mold impurity is carried out into n mold well field 13 and an epitaxial layer 29 by the self aryne.
[0259] Consequently, in p mold well field 12 and an epitaxial layer 21, the high-concentration impurity range 19 deeper than the extension field 20 and, i.e., n mold source / drain field, is formed, and the high-concentration impurity range 27 deeper than the extension field 28 and, i.e., p mold source / drain field, is formed in n mold well field 13 and an epitaxial layer 29.
[0260] Moreover, for example, refractory metal film (a tungsten, titanium, etc.) is formed with a CVD method on an epitaxial layer 21 and the whole surface of the silicon substrate 11 including 29 tops. Then, if annealing is performed

(like a heat process), an epitaxial layer 21, and the silicon and the refractory metal film in 29 will react chemically, and the refractory metal silicide layers 22 and 30 will be formed in the upper part of epitaxial layers 21 and 29.
[0261] Then, the unreacted refractory metal film is removed.
[0262] According to the above process, MOSFET which has the EREBETEDDO source / drain structure is completed.
[0263] Drawing 33 shows the semiconductor device in connection with the gestalt of the 5th operation of this invention.
[0264] This semiconductor device is related with MOSFET formed in an epitaxial layer.
[0265] In the single crystal silicon substrate 11, the isolation insulator layer 14 of STI structure is formed. On the isolation insulator layer 14, the stopper insulator layer 35 which has width of face narrower than the width of face of the isolation insulator layer 14 is formed. The width of face of the stopper insulator layer 35 is set as the minimum isolation width of face a demanded on a property.
[0266] Epitaxial layers 21 and 29 are formed on a silicon substrate 11. Epitaxial layers 21 and 29 are formed also on the isolation insulator layer 14. However, epitaxial layers 21 and 29 are mutually separated by the stopper insulator layer 35. The height (thickness) of epitaxial layers 21 and 29 is the same as the height of the stopper insulator layer 35, or since it is set up lower than it, it is separated only from the minimum isolation width of face a demanded on a property of epitaxial layers 21 and 29.
[0267] p mold well field 12 is formed in an epitaxial layer 21 and a silicon substrate 11, and n mold well field 13 is formed in an epitaxial layer 29 and a silicon substrate 11.
[0268] The n channel mold MOSFET is formed on p mold well field 12 (on an epitaxial layer 21).
[0269] That is, on p mold well field 12, the polish recon film (gate electrode) 16 containing silicon oxide (gate dielectric film) 15 and an impurity is formed. On the polish recon film 16, the silicon oxide (cap oxide film) 17 used as the mask at the time of processing the polish recon film 16 is formed. Moreover, the silicon nitride (side-attachment-wall insulator layer) 18 is formed in the side attachment wall of the polish recon film 16.
[0270] In p mold well field 12, low-concentration n mold extension field 20 is formed rather than n mold source / drain field 19, and this the source / drain field 19. That is, the source / drain field 19 is formed in p mold well field 12 of the both sides of the polish recon film 16, and n mold extension field 20 is formed in p mold well field [directly under] 12 of the silicon nitride 18.
[0271] A part of base of the source / drain field 19 touches the isolation insulator layer 14. Therefore, the plane-of-composition product of p mold well field 12, and the n mold source / drain field 19 can be made small, and the parasitic capacitance of the source / drain field 19 can be reduced.
[0272] Similarly, the p channel mold MOSFET is formed on n mold well field 13 (on an epitaxial layer 29).
[0273] That is, on n mold well field 13, the polish recon film (gate electrode) 24 containing silicon oxide (gate dielectric film) 23 and an impurity is formed. On the polish recon film 24, the silicon oxide (cap oxide film) 25 used as the mask at the time of processing the polish recon film 24 is formed. Moreover, the silicon nitride (side-attachment-wall insulator layer) 26 is formed in the side attachment wall of the polish recon film 24.
[0274] In n mold well field 13, low-concentration p mold extension field 28 is formed rather than p mold source / drain field 27, and this the source / drain field 27. That is, the source / drain field 27 is formed in n mold well field 13 of the both sides of the polish recon film 24, and p mold extension field 28 is formed in n mold well field [directly under] 13 of the silicon nitride 26.
[0275] A part of base of the source / drain field 27 touches the isolation insulator layer 14. Therefore, the plane-of-composition product of n mold well field 13, and the p mold source / drain field 27 can be made small, and the parasitic capacitance of the source / drain field 27 can be reduced.
[0276] Next, the manufacture approach of the semiconductor device of the gestalt the 5th above-mentioned operation is explained.
[0277] First, as shown in drawing 34 , the isolation insulator layer 14 of STI structure is formed in the single crystal silicon substrate 11. Moreover, for example, the stopper insulator layer 35 is formed on [whole] a silicon substrate 11 with a CVD method. Although the stopper insulator layer 35 may be constituted from what kind of thing as long as it is an ingredient which has insulation, a silicon nitride, its silicon oxide, etc. are realistic, for example.
[0278] Moreover, PEP (photo-etching process) is performed and the resist film which has width of face narrower than the width of face of the isolation insulator layer 14 is formed on the stopper insulator layer 35 on the isolation insulator layer 14. This resist film is used as a mask, by RIE, the stopper insulator layer 35 is etched and the stopper insulator layer 35 is formed on the isolation insulator layer 14. Then, the resist film exfoliates.
[0279] In this example, the width of face of the stopper insulator layer 35 is the minimum isolation width of face a demanded on a property.

[0280] Next, as shown in drawing 35 , epitaxial layers (single-crystal-silicon layer) 21 and 29 are alternatively formed with selection epitaxial growth on the silicon substrate 11 which became unreserved. In selection epitaxial growth, material gas, membrane formation temperature, etc. are adjusted and a silicon epitaxial layer is formed only on a silicon substrate 11.
[0281] In addition, be [epitaxial layers 21 and 29 / isotropic], i.e., in order to grow up to be a lengthwise direction and a longitudinal direction, epitaxial layers 21 and 29 are formed also on the isolation insulator layer 14.
[0282] When the height from the front face of a silicon substrate 11 to the top face of the stopper insulator layer 35, i.e., the front face of the isolation insulator layer 14 and the front face of a silicon substrate 11, is substantially equal, the height of epitaxial layers 21 and 29 is the same as the height of the stopper insulator layer 35, or it is adjusted so that it may become lower than it.
[0283] Next, as shown in drawing 36 , with ion-implantation, in an epitaxial layer 21 and a silicon substrate 11, the ion implantation of the p mold impurity is carried out, p mold well field 12 is formed, and in an epitaxial layer 29 and a silicon substrate 11, the ion implantation of the n mold impurity is carried out, and n mold well field 13 is formed.
[0284] Then, for example, by the oxidizing [thermally] method, silicon oxide (gate oxide) 15 is formed on p mold well field 12, and silicon oxide (gate oxide) 23 is formed on n mold well field 13.
[0285] Moreover, for example, silicon oxide 15 and the polish recon film 16 and 24 which contained the impurity on 23 are formed using a CVD method. Silicon oxide (cap oxide film) 17 and 25 is formed on the polish recon film 16 and 24 with a CVD method continuing. Then, patterning of the silicon oxide 17 and 25 is carried out, further, these silicon oxide 17 and 25 is used as a mask, by RIE, the polish recon film 16 and 24 is etched and the gate electrode of MOSFET is formed.
[0286] Moreover, using ion-implantation, the polish recon film (gate electrode) 16 is used as a mask, and the ion implantation of the n mold impurity is carried out into p mold well field 12 by the self aryne. Consequently, in p mold well field 12, shallow and low-concentration n mold impurity range 20, i.e., n mold extension field, is formed.
[0287] Similarly, using ion-implantation, the polish recon film (gate electrode) 24 is used as a mask, and the ion implantation of the p mold impurity is carried out into n mold well field 13 by the self aryne. Consequently, in n mold well field 13, shallow and low-concentration p mold impurity range 28, i.e., p mold extension field, is formed.
[0288] Then, it oxidizes thermally and silicon oxide is formed in the front face of the polish recon film (gate electrode) 16 and 24.
[0289] Moreover, for example, the silicon nitrides 18 and 26 which cover completely the polish recon film (gate electrode) 16 and 24 on [whole] the isolation insulator layer 14 and a component field are formed with a CVD method. Moreover, the silicon nitrides 18 and 26 are etched and these silicon nitrides 18 and 26 are made to remain only on the side attachment wall of the polish recon film 16 and 24 by RIE.
[0290] Next, using ion-implantation, the polish recon film 16 and the silicon nitride 18 are used as a mask, and the ion implantation of the n mold impurity is carried out into p mold well field 12 by the self aryne. Moreover, using ion-implantation, the polish recon film 24 and the silicon nitride 26 are used as a mask, and the ion implantation of the p mold impurity is carried out into n mold well field 13 by the self aryne.
[0291] Consequently, in p mold well field 12, the high-concentration impurity range 19 deeper than n mold extension field 20 and, i.e., n mold source / drain field, is formed, and the high-concentration impurity range 27 deeper than p mold extension field 28 and, i.e., p mold source / drain field, is formed in n mold well field 13.
[0292] Of the above process, it is formed in an epitaxial layer 21 and 29, and MOSFET to which a part of base of the source / drain fields 19 and 27 contacts the isolation insulator layer 14 is completed.
[0293] Drawing 37 shows the semiconductor device in connection with the gestalt of the 6th operation of this invention.
[0294] The semiconductor device of the gestalt of this operation is the modification of the semiconductor device in connection with the gestalt of the 1st operation of drawing 1 , and the description arranges the stopper insulator layer 35 on the isolation insulator layer 14 in the component isolation region A, and is that it does not arrange the stopper insulator layer 35 on the isolation insulator layer 14 in the component isolation region B.
[0295] In this case, in the component isolation region B, an epitaxial layer 29 is formed so that the isolation insulator layer 14 may be straddled. Namely, MOSFET The source / drain field 27a, and MOSFET of T1 The source / drain field 27b of T2 will be connected electrically.
[0296] The semiconductor device of the gestalt of this operation is MOSFET. T1 and MOSFET It faces connecting T2 electrically and can contribute to the improvement in a degree of integration of a component compared with the case where the wiring layer formed in the upper layer of MOSFET is used. That is, with the semiconductor device of the gestalt of this operation, it is MOSFET. The contact field to the source / drain field becomes unnecessary about the

electrical installation of T1 and T2.
[0297] Drawing 38 shows the semiconductor device in connection with the gestalt of the 7th operation of this invention.
[0298] The semiconductor device of the gestalt of this operation is the modification of the semiconductor device in connection with the gestalt of the 5th operation of drawing 33 , and the description is in the point that the stopper insulator layer 35 is not arranged on the isolation insulator layer 14 in the component isolation region B.
[0299] In this case, epitaxial layer 29a and epitaxial layer 29b are mutually combined on the isolation insulator layer 14 of the component isolation region B. Namely, the source / drain field 27a, and MOSFET of MOSFETT1 The source / drain field 27b of T2 will be connected electrically.
[0300] The semiconductor device of the gestalt of this operation is MOSFET. T1 and MOSFET It faces connecting T2 electrically and can contribute to the improvement in a degree of integration of a component compared with the case where the wiring layer formed in the upper layer of MOSFET is used. That is, with the semiconductor device of the gestalt of this operation, it is MOSFET. The contact field to the source / drain field becomes unnecessary about the electrical installation of T1 and T2.
[0301] Drawing 39 and drawing 40 show the technique applied in case the semiconductor device of drawing 37 and drawing 38 is manufactured.
[0302] With selection epitaxial growth, this technique grows up epitaxial layers 29a and 29b from a silicon substrate 11, and combines mutually these epitaxial layers 29a and 29b on the isolation insulator layer 14.
[0303] In this technique, supposing growth of epitaxial layers 29a and 29b is performed isotropic, when width of face of the isolation insulator layer 14 is set to H, it is necessary to form epitaxial layers 29a and 29b by H/2 or more thickness.
[0304] Drawing 41 shows the situation when forming a contact hole to the contact field of the epitaxial layer on an isolation insulator layer.
[0305] Formation of a contact hole 39 is performed by PEP (photo-etching process) and the etching process. However, in PEP, usually it may double between a mask (reticle) and a wafer (silicon substrate), a gap may arise, and the location of a contact hole 39 may shift from the contact field of an epitaxial layer 21.
[0306] In this case, of an etching process, if a contact hole 39 is formed in an interlayer insulation film 31, trench 39a will be formed in the isolation insulator layer 14. This usually consists of ingredients (for example, silicon oxide) with same isolation insulator layer 14 and interlayer insulation film 31, and the isolation insulator layer 14 is because it does not have etch selectivity to an interlayer insulation film 31.
[0307] If trench 39a formed in the isolation insulator layer 14 is attained to a silicon substrate 11, it will generate the leakage current from the source / drain field to the well field 12. Moreover, by the spatter, in case this trench 39a forms barrier metal in a contact hole 39, it produces poor membrane formation of barrier metal.
[0308] In order to avoid such a situation, even if it doubles between a mask and a wafer and a gap arises, the layout which gave sufficient margin width for the contact field of an epitaxial layer is needed so that a contact hole may not separate from the contact field of an epitaxial layer. However, this margin width has a bad influence on improvement in the degree of integration of a component.
[0309] Then, he forms the etching stopper layer 40 beforehand on the silicide layer 22 (epitaxial layer 21) and the isolation insulator layer 14, and is trying to stop advance of etching in the etching stopper layer 40 conventionally, at the time of formation of a contact hole 39, as shown in drawing 42 .
[0310] Since the etching stopper layer 40 stops advance of etching, it consists of ingredients (for example, silicon nitride) which have etch selectivity to the isolation insulator layer 14 and an interlayer insulation film 31.
[0311] Therefore, a contact hole 39 can be formed, without forming a trench in the isolation insulator layer 14, if etching removes only the etching stopper layer 40 of the pars basilaris ossis occipitalis of a contact hole 39 after forming a contact hole 39 (field self aryne contact).
[0312] By the way, as shown in drawing 43 , in the case of this invention, on the isolation insulator layer 14, the stopper insulator layer 35 which makes growth of the longitudinal direction of the epitaxial layer 21 at the time of selection epitaxial growth stop is formed.
[0313] Then, if this stopper insulator layer 35 is constituted from an ingredient (for example, silicon nitride) which has etch selectivity to the isolation insulator layer 14 and an interlayer insulation film 31, advance of etching can be stopped by the stopper insulator layer 35 at the time of formation of a contact hole 39.
[0314] That is, since according to this invention a trench is not formed in the isolation insulator layer 14 even if it does not prepare an etching stopper layer at the time of formation of a contact hole 39, field self aryne contact is realizable without an etching stopper layer.

[0315] Next, the manufacture approach applicable to the semiconductor device (thing about MOSFET which has the EREBETEDDO source / drain structure) of the gestalt of the above-mentioned 1st thru/or the 4th above-mentioned operation is explained.
[0316] By the manufacture approach in the gestalt of each operation mentioned above, the stopper insulator layer 35 was manufactured according to the original process. In this example, the formation process of the stopper insulator layer 35 is included in other processes (formation process of a side-attachment-wall insulator layer), and reduction of the number of production processes is aimed at.
[0317] First, as shown in drawing 44 , the isolation insulator layer 14 of STI structure is formed in the single crystal silicon substrate 11. Moreover, p mold well field 12 and n mold well field 13 are formed in a silicon substrate 11, and silicon oxide (gate oxide) 15 and 23 is formed on the component field enclosed by the isolation insulator layer 14.
[0318] Moreover, as usual, on p mold well field 12, the polish recon film (gate electrode) 16 and silicon oxide (cap oxide film) 17 are formed, and the polish recon film (gate electrode) 24 and silicon oxide (cap oxide film) 25 are formed on n mold well field 13.
[0319] Next, as shown in drawing 45 , in p mold well field 12, shallow and low-concentration n mold impurity range 20, i.e., n mold extension field, is formed, and shallow and low-concentration p mold impurity range 28, i.e., p mold extension field, is formed in n mold well field 13.
[0320] Then, an insulator layer (for example, silicon nitride) 41 is formed the whole surface on a silicon substrate 11. Moreover, PEP (photo-etching process) is performed and the resist film 42 is formed on the insulator layer 41 on the isolation insulator layer 14. After using the resist film 42 as a mask and etching an insulator layer 41 by anisotropic etching, the resist film 42 is removed.
[0321] Consequently, as shown in drawing 46 , an insulator layer 41 remains on the side attachment wall of the polish recon film (gate electrode) 16 and 24, and the isolation insulator layer 14. The insulator layer 41 of the side attachment wall of the polish recon film 16 and 24 turns into a side-attachment-wall insulator layer used as the mask at the time of forming the source / drain field, and the insulator layer 41 on the isolation insulator layer 14 (35) turns into a stopper insulator layer.
[0322] Then, the silicon oxide 15 and 23 which exists in the both sides of the polish recon film 16 and 24 is removed, and selection epitaxial growth is performed. Moreover, formation of the source / drain field, and a silicide layer completes MOSFET which has the EREBETEDDO source / drain structure.
[0323] By such manufacture approach, since the side-attachment-wall insulator layer and stopper insulator layer of a gate electrode are formed in coincidence, compared with the former, the increment in the number of production processes is suppressed.
[0324] Drawing 47 and drawing 48 show the semiconductor device in connection with the gestalt of the 8th operation of this invention.
[0325] The example of amelioration of the semiconductor device in connection with the gestalt of the 2nd operation of drawing 6 in drawing 47 and drawing 48 are the examples of amelioration of the semiconductor device in connection with the gestalt of the 5th operation of drawing 33 , and it enables it to acquire the same effectiveness as the semiconductor device of the gestalt of the 2nd and 5th operations by changing the configuration of the isolation insulator layer 14, without using a stopper insulator layer.
[0326] The description of this semiconductor device establishes a hollow in the edge of the isolation insulator layer 14, and is in the point of having made it an isolation insulator layer serve as a convex type. Epitaxial layers 21 and 29 are formed on a silicon substrate 11 and in the hollow of the isolation insulator layer 14, and do not exceed the heights of the isolation insulator layer 14.
[0327] That is, the heights of the isolation insulator layer 14 have the almost same function as a stopper insulator layer, and make late substantially the speed of advance of growth of the longitudinal direction of epitaxial layers 21 and 29. Therefore, the isolation width of face a which epitaxial layers 21 and 29 do not connect too hastily after growth of epitaxial layers 21 and 29, and is demanded on a property is securable.
[0328] Moreover, in the semiconductor device of the gestalt of this operation, since the stopper insulator layer is unnecessary, while a production process is simplified, in case heights are formed in the isolation insulator layer 14, it is not necessary to take into consideration a doubling gap which is produced at the time of patterning of a stopper insulator layer.
[0329] Drawing 49 thru/or drawing 51 show the technique applied in case the semiconductor device of drawing 47 and drawing 48 is manufactured.
[0330] This technique forms a slot in the edge of the isolation insulator layer 14, and uses the isolation insulator layer 14 as a convex type.

[0331] First, as shown in drawing 49 , the isolation insulator layer (for example, silicon oxide) 14 of STI structure is formed in the single crystal silicon substrate 11. The front face of the isolation insulator layer 14 shall be in general equal on the surface of a silicon substrate.
[0332] Next, as shown in drawing 50 , wet etching of the isolation insulator layer 14 is performed using NH4 F. Generally, since the direction of a edge becomes high compared with the center section of the isolation insulator layer 14, the etching rate of the isolation insulator layer 14 becomes depressed in the edge of the isolation insulator layer 14 by the wet etching of the isolation insulator layer 14 (slot), and 43 is formed.
[0333] Next, as shown in drawing 51 , epitaxial layers (single-crystal-silicon layer) 21 and 29 are alternatively formed on a silicon substrate 11 with selection epitaxial growth. The tip at this time, for example, the longitudinal direction of an epitaxial layer 21, moves in a path as shown in an arrow head in the isolation insulator layer 14 top. That is, the distance which the tip of an epitaxial layer 21 moves from a silicon substrate 11 to the heights of the isolation insulator layer 14 becomes longer than the case where there is no direction fang furrow in case there is a slot.
[0334] Therefore, the isolation width of face a which can prevent the situation which epitaxial layers 21 and 29 short-circuit after growth of epitaxial layers 21 and 29, and is demanded on a property is securable.
[0335] Moreover, since the stopper insulator layer is unnecessary, while a production process is simplified, since the heights of the isolation insulator layer 14 are formed in self align, they do not need to take into consideration a doubling gap which is produced at the time of patterning of a stopper insulator layer.
[0336] Drawing 52 and drawing 53 show the formation process of an isolation insulator layer applicable to MOSFET (it corresponds to the gestalt of the 1st thru/or the 4th operation) which has the EREBETEDDO source / drain structure.

[0337] First, for example, sequential formation of silicon oxide 44 and the silicon nitride 45 is carried out on the single crystal silicon substrate 11 using a CVD method. By PEP (photo-etching process), a resist pattern is formed, this resist pattern is used as a mask, and the silicon nitride 45 is etched by RIE.
[0338] Moreover, after removing a resist pattern, the silicon nitride 45 is used as a mask, by RIE, silicon oxide 44 and a silicon substrate 11 are etched, and a trench is formed in a silicon substrate 11.
[0339] Moreover, silicon oxide which embeds a trench completely on the silicon nitride 45 is formed. And by CMP, this silicon oxide is ground and etched, only in a trench, silicon oxide is made to remain and the isolation insulator layer 14 of STI structure is formed.
[0340] Then, silicon oxide 44 and the silicon nitride 45 are removed.
[0341] According to the formation process of the above-mentioned isolation insulator layer 14, the top face of the isolation insulator layer 14 is higher than the front face of a silicon substrate 11. For this reason, the same function as the stopper insulator layer which makes the heights of this isolation insulator layer 14 stop growth of the longitudinal direction of an epitaxial layer can be given.
[0342] However, after forming the isolation insulator layer 14, the gate electrode of MOSFET is formed on a silicon substrate (component field) 11 and the isolation insulator layer (component isolation region) 14. That is, if the isolation insulator layer 14 has projected from the silicon substrate 11, the level difference section will arise on the boundary of a silicon substrate 11 and the isolation insulator layer 14, and processing of the gate electrode of MOSFET will become very difficult in this level difference section.
[0343] So, in the semiconductor device of the gestalt of the above-mentioned 1st thru/or the 4th above-mentioned operation, the top face of the isolation insulator layer 14 is made in general equal to the front face of a silicon substrate 11, the gate electrode of MOSFET is formed in this condition, a stopper insulator layer is prepared on the isolation insulator layer 14 after this, and selection epitaxial growth is performed.
[0344]
[Effect of the Invention] As mentioned above, as explained, according to the semiconductor device of this invention, growth of the longitudinal direction of the epitaxial layer at the time of selection epitaxial growth can be prevented now by the stopper insulator layer arranged on an isolation insulator layer. That is, since a stopper insulator layer has a function as a wall which prevents growth of the longitudinal direction of an epitaxial layer, only the width of face of a stopper insulator layer can secure isolation width of face at worst.
[0345] Therefore, while being able to acquire sufficient isolation property, it becomes, without the components which adjoin mutually short-circuiting. Moreover, improvement in the degree of integration of a component and contraction of a chip size can be aimed at.
[0346] Moreover, when not arranging a stopper insulator layer on an isolation insulator layer, the components which adjoin mutually on an isolation insulator layer can be electrically connected by the epitaxial layer.
[0347] Moreover, a trench is not formed in an isolation insulator layer at the time of contact hole formation with

constituting a stopper insulator layer from an ingredient which has etch selectivity to an isolation insulator layer.
[0348] Furthermore, even if it does not prepare a stopper insulator layer on an isolation insulator layer, the same effectiveness as the case where a stopper insulator layer is prepared can be acquired by forming a slot in the edge section of an isolation insulator layer, and using an isolation insulator layer as a convex type.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The sectional view showing the semiconductor device in connection with the gestalt of the 1st operation of this invention.
[Drawing 2] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 1 .
[Drawing 3] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 1 .
[Drawing 4] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 1 .
[Drawing 5] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 1 .
[Drawing 6] The sectional view showing the semiconductor device in connection with the gestalt of the 2nd operation of this invention.
[Drawing 7] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 6 .
[Drawing 8] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 6 .
[Drawing 9] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 6 .
[Drawing 10] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 6 .
[Drawing 11] Drawing showing the relation of the height of epitaxial layer thickness and a stopper insulator layer.
[Drawing 12] Drawing showing the relation of the height of epitaxial layer thickness and a stopper insulator layer.
[Drawing 13] Drawing showing the relation of the height of epitaxial layer thickness and a stopper insulator layer.
[Drawing 14] The top view showing the semiconductor device in connection with the gestalt of the 3rd operation of this invention.
[Drawing 15] The sectional view which meets the XV-XV line of drawing 14 .
[Drawing 16] The top view showing one process of the manufacture approach of the semiconductor device of drawing 14 .
[Drawing 17] The sectional view which meets the XVII-XVII line of drawing 16 .
[Drawing 18] The top view showing one process of the manufacture approach of the semiconductor device of drawing 14 .
[Drawing 19] The sectional view which meets the XIX-XIX line of drawing 18 .
[Drawing 20] The top view showing one process of the manufacture approach of the semiconductor device of drawing 14 .
[Drawing 21] The sectional view which meets the XXI-XXI line of drawing 20 .
[Drawing 22] The top view showing the semiconductor device in connection with the gestalt of the 4th operation of this invention.
[Drawing 23] The sectional view which meets the XXIII-XXIII line of drawing 22 .
[Drawing 24] The sectional view which meets the XXIV-XXIV line of drawing 22 .
[Drawing 25] The top view showing one process of the manufacture approach of the semiconductor device of drawing 22 .

[Drawing 26] The sectional view which meets the XXVI-XXVI line of drawing 25 .
[Drawing 27] The top view showing one process of the manufacture approach of the semiconductor device of drawing 22 .
[Drawing 28] The sectional view which meets the XXVIII-XXVIII line of drawing 27 .
[Drawing 29] The sectional view which meets the XXIX-XXIX line of drawing 27 .
[Drawing 30] The top view showing one process of the manufacture approach of the semiconductor device of drawing 22 .
[Drawing 31] The sectional view which meets XXXI-XXXI line of drawing 30 .
[Drawing 32] The sectional view which meets XXXII-XXXII line of drawing 30 .
[Drawing 33] The sectional view showing the semiconductor device in connection with the gestalt of the 5th operation of this invention.
[Drawing 34] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 33 .
[Drawing 35] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 33 .
[Drawing 36] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 33 .
[Drawing 37] The sectional view showing the semiconductor device in connection with the gestalt of the 6th operation of this invention.
[Drawing 38] The sectional view showing the semiconductor device in connection with the gestalt of the 7th operation of this invention.
[Drawing 39] Drawing showing one process of the manufacture approach applicable to the semiconductor device of drawing 37 and drawing 38 .
[Drawing 40] Drawing showing one process of the manufacture approach applicable to the semiconductor device of drawing 37 and drawing 38 .
[Drawing 41] Drawing showing the trouble at the time of contact hole formation.
[Drawing 42] Drawing showing the example which solved the trouble of drawing 41 with the etching stopper.
[Drawing 43] Drawing showing the example which solved the trouble of drawing 41 by the stopper insulator layer.
[Drawing 44] Drawing showing one process of the manufacture approach applicable to the equipment of the gestalt of the 1st thru/or the 4th operation.
[Drawing 45] Drawing showing one process of the manufacture approach applicable to the equipment of the gestalt of the 1st thru/or the 4th operation.
[Drawing 46] Drawing showing one process of the manufacture approach applicable to the equipment of the gestalt of the 1st thru/or the 4th operation.
[Drawing 47] The sectional view showing the semiconductor device in connection with the gestalt of the 8th operation of this invention.
[Drawing 48] The sectional view showing the semiconductor device in connection with the gestalt of the 8th operation of this invention.
[Drawing 49] Drawing showing one process of the manufacture approach applicable to the semiconductor device of drawing 47 and drawing 48 .
[Drawing 50] Drawing showing one process of the manufacture approach applicable to the semiconductor device of drawing 47 and drawing 48 .
[Drawing 51] Drawing showing one process of the manufacture approach applicable to the semiconductor device of drawing 47 and drawing 48 .
[Drawing 52] The sectional view showing the formation process of the isolation insulator layer of STI structure.
[Drawing 53] The sectional view showing the formation process of the isolation insulator layer of STI structure.
[Drawing 54] The sectional view showing the conventional semiconductor device.
[Drawing 55] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 54 .
[Drawing 56] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 54 .
[Drawing 57] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 54 .
[Drawing 58] The sectional view showing one process of the manufacture approach of the semiconductor device of

drawing 54 .
[Drawing 59] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 54 .
[Drawing 60] Drawing showing the conventional semiconductor device.
[Drawing 61] Drawing showing the semiconductor device of the EREBETEDDO source / drain structure.
[Drawing 62] Drawing showing the fault of the conventional semiconductor device.
[Drawing 63] Drawing showing the advantage of the semiconductor device of the EREBETEDDO source / drain structure.
[Drawing 64] The sectional view showing the conventional semiconductor device.
[Drawing 65] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 64 .
[Drawing 66] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 64 .
[Drawing 67] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 64 .
[Drawing 68] The sectional view showing one process of the manufacture approach of the semiconductor device of drawing 64 .
[Drawing 69] Drawing showing the advantage of the conventional semiconductor device.
[Drawing 70] Drawing showing the fault of the conventional semiconductor device.
[Drawing 71] Drawing showing the fault of the conventional semiconductor device.
[Description of Notations]
11 [ ] : -- Single Crystal Silicon Substrate,
12 [ ] : -- P Mold Well Field,
13 [ ] : -- N Mold Well Field,
14 [ ] : -- Isolation Insulator Layer,
15 23 : Silicon oxide (gate dielectric film),
16 24 : Polish recon film (gate electrode),
17 25 : Silicon oxide (cap oxide film),
18, 26, 41 : Silicon nitride (side-attachment-wall insulator layer),
19 [ ] : -- N Mold Source / Drain Field,
20 [ ] : -- N Mold Extension Field,
21 [ ] : -- Epitaxial Layer (N Mold Source / Drain Field),
27 [ ] : -- P Mold Source / Drain Field,
28 [ ] : -- P Mold Extension Field,
29 [ ] : -- Epitaxial Layer (P Mold Source / Drain Field),
22 30 : Refractory metal silicide layer,
31 [ ] : -- Interlayer Insulation Film,
32a, 32b : Contact plug,
33a, 33b : Wiring,
34 [ ] : -- Passivation Film,
35 [ ] : -- Stopper Insulator Layer,
36 42 : Resist film,
37, 38, 39 : Contact hole,
40 [ ] : -- an etching stopper layer.
43 [ ] : -- Becoming Depressed
44 [ ] : -- Silicon Oxide,
45 [ ] : -- a silicon nitride.

[Translation done.]

* NOTICES *

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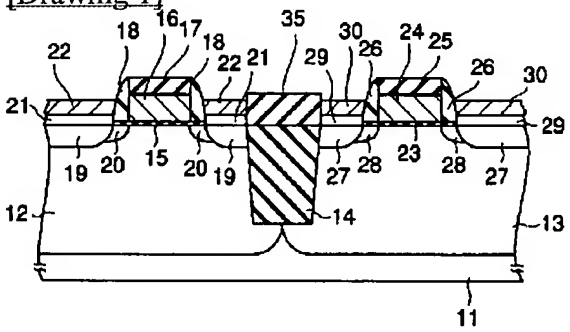
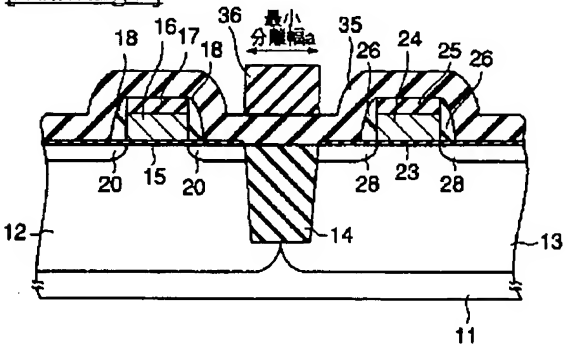
DRAWINGS

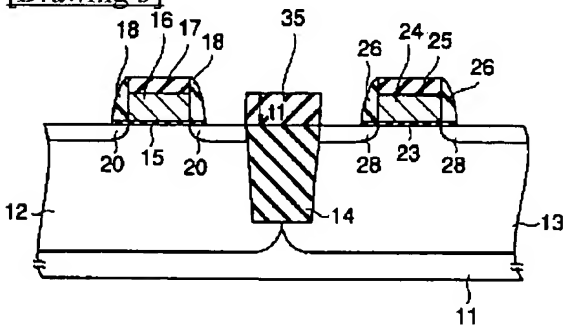
[Drawing 1]



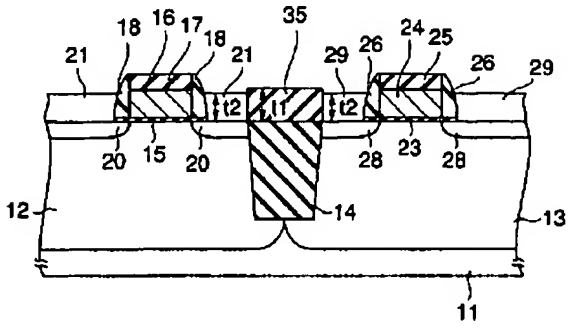
[Drawing 2]



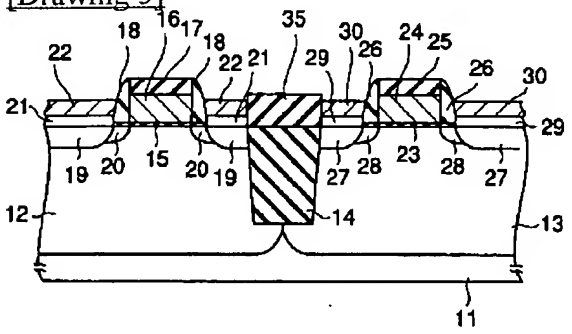
[Drawing 3]



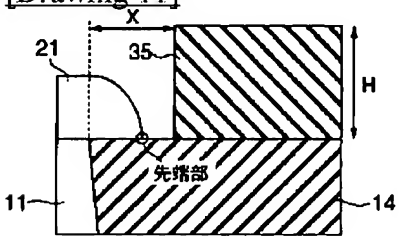
[Drawing 4]



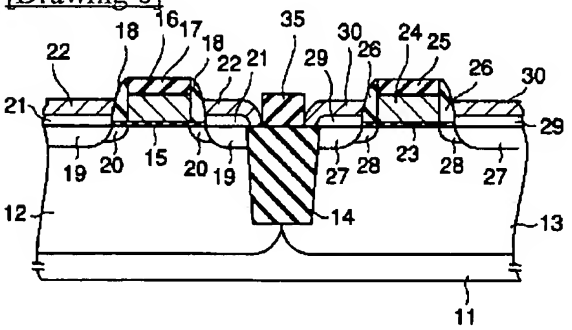
[Drawing 5]



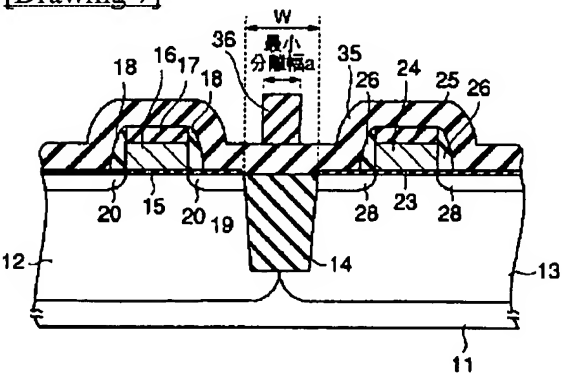
[Drawing 11]



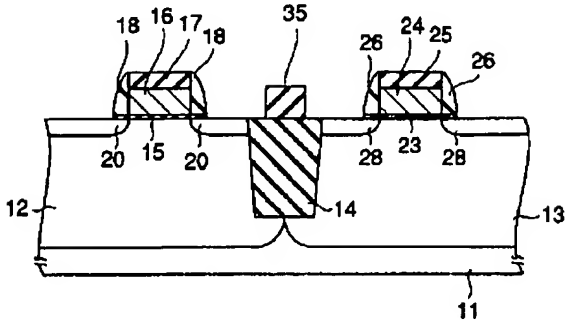
[Drawing 6]



[Drawing 7]



[Drawing 8]



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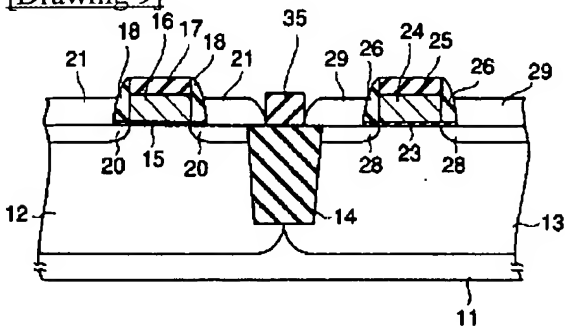

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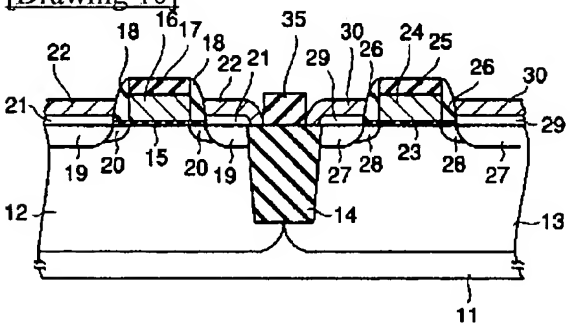
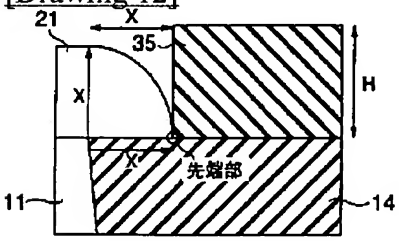


[Drawing 12]



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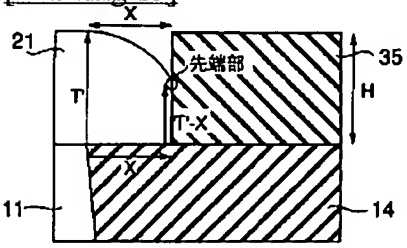
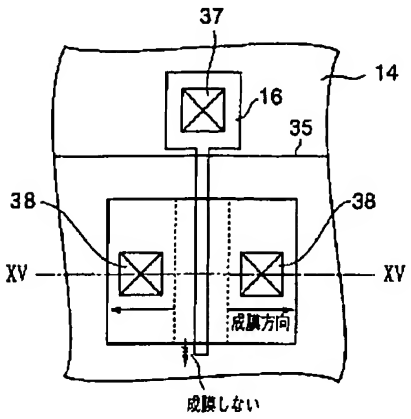


[Drawing 14]



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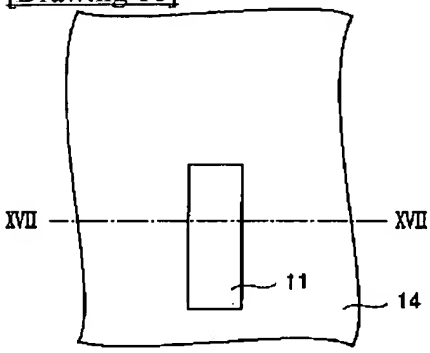

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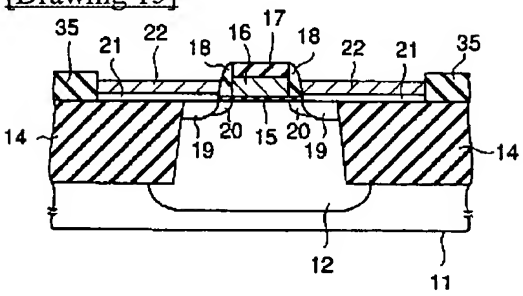

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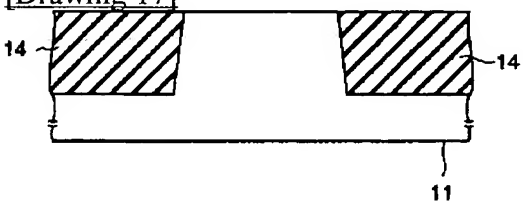
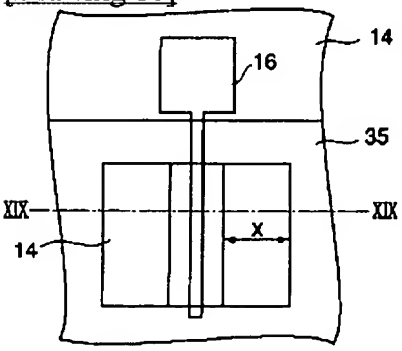
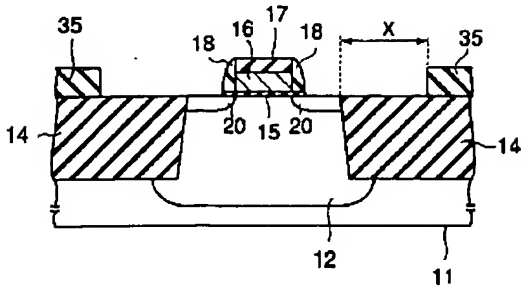


[Drawing 18]



[Drawing 19]



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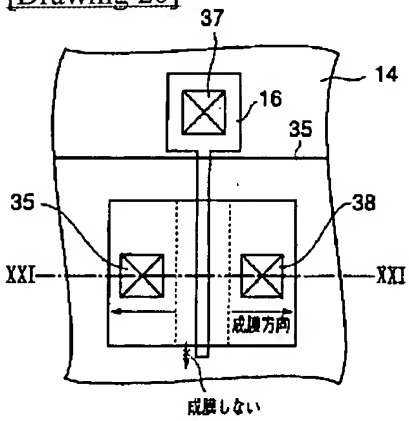

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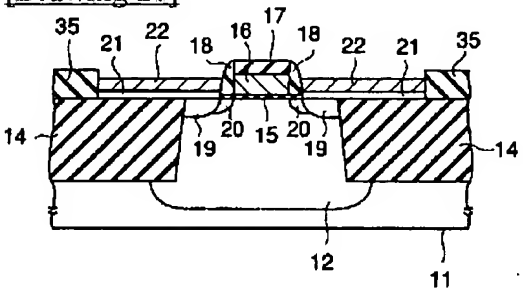

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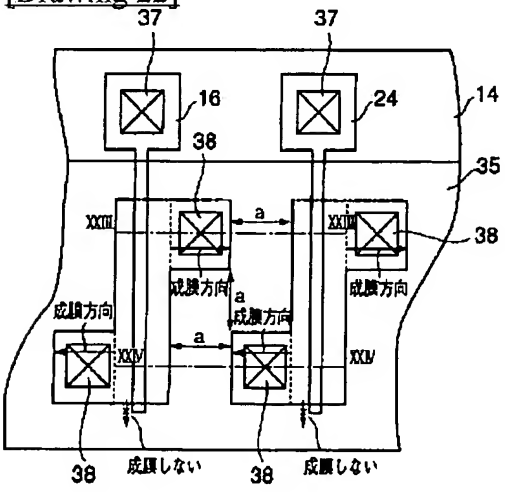
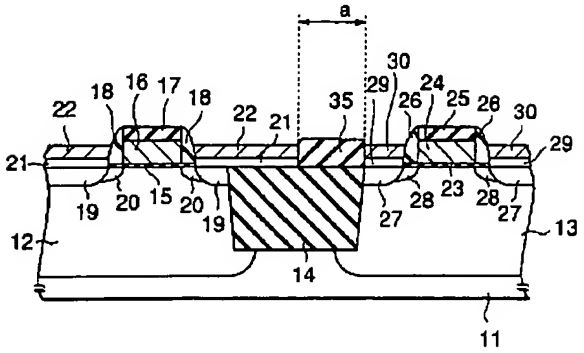


[Drawing 23]



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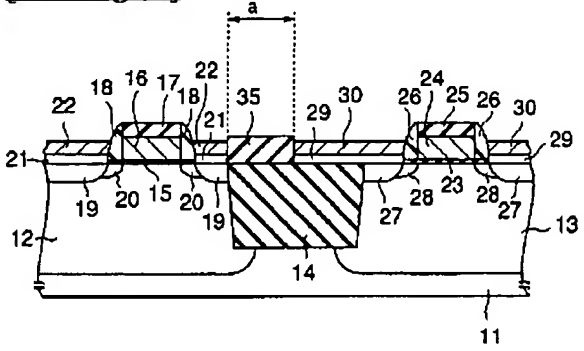

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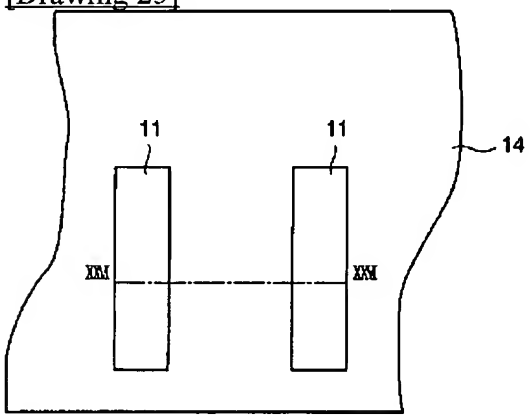

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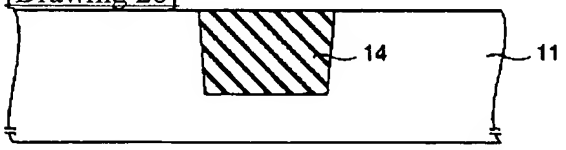

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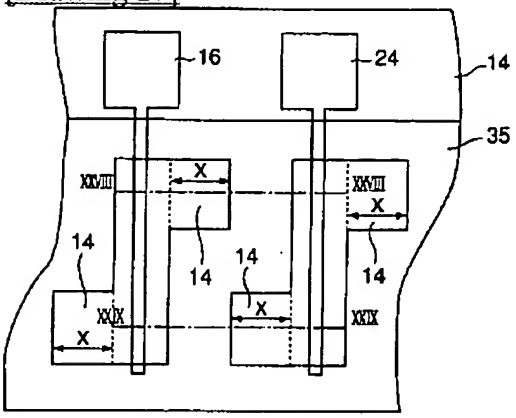

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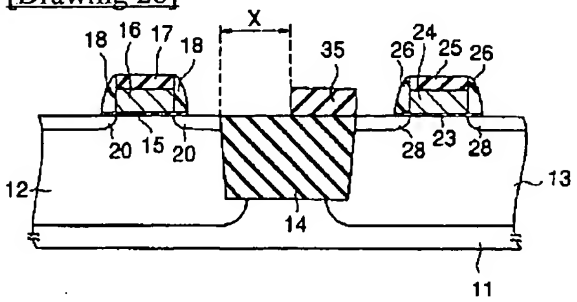

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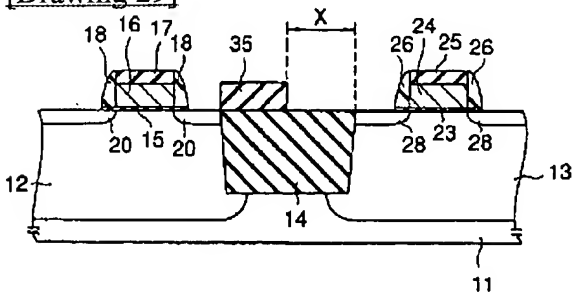

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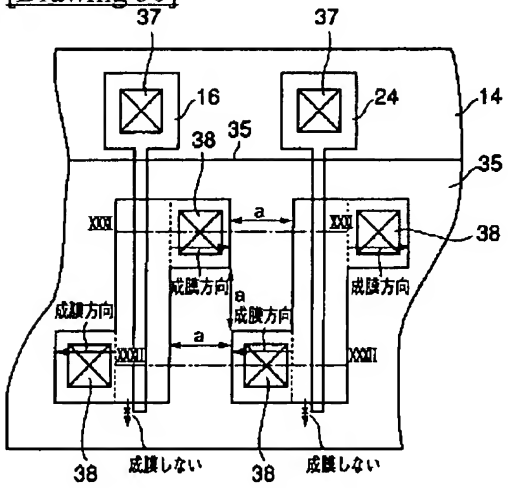

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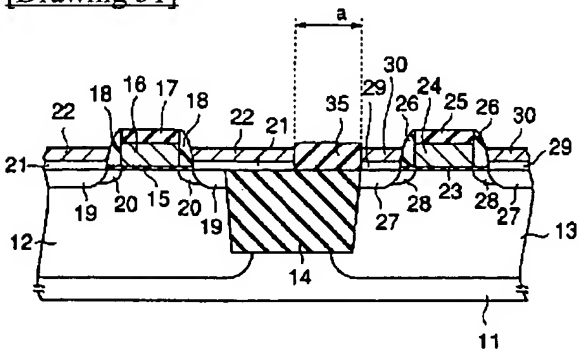

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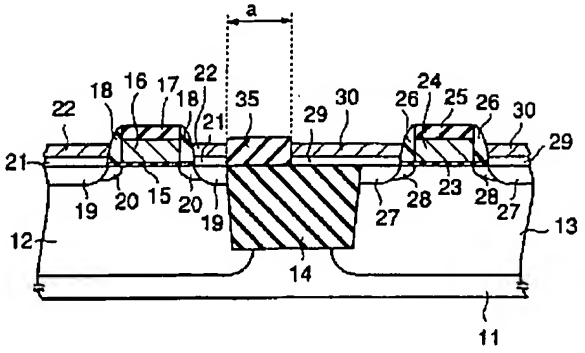

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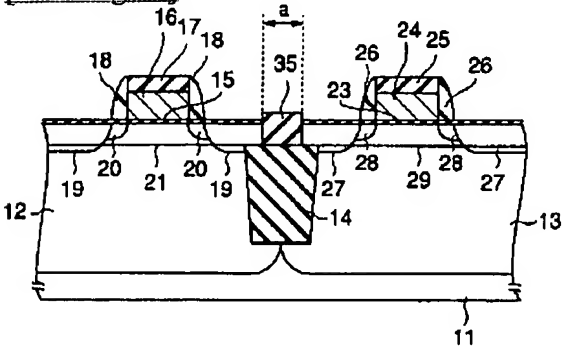

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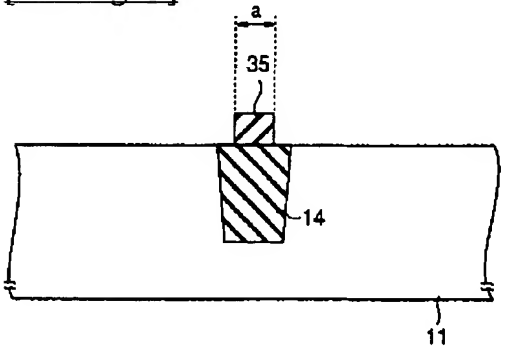

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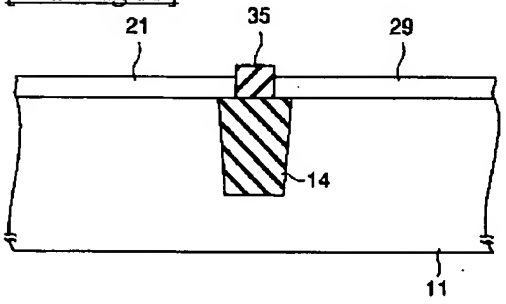

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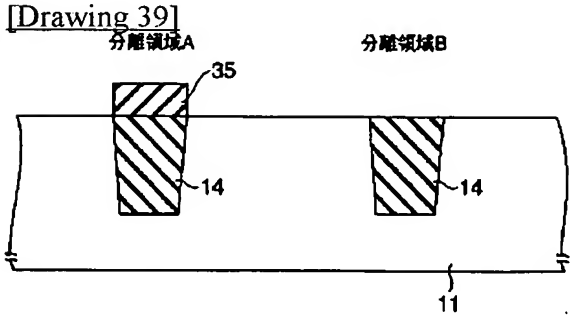

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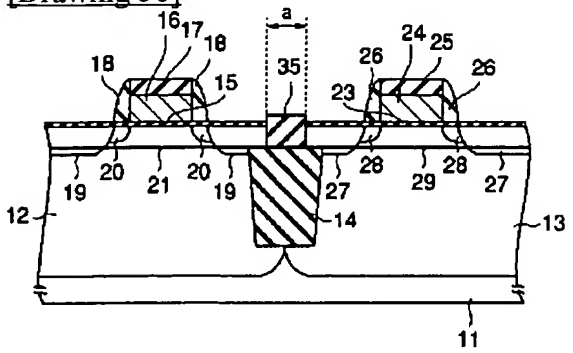

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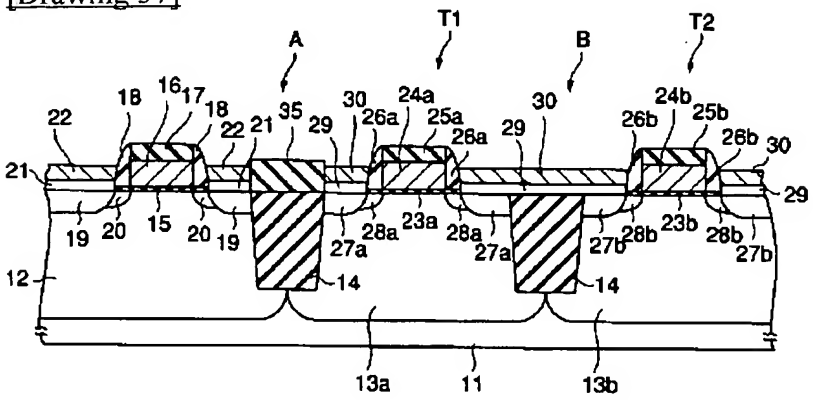

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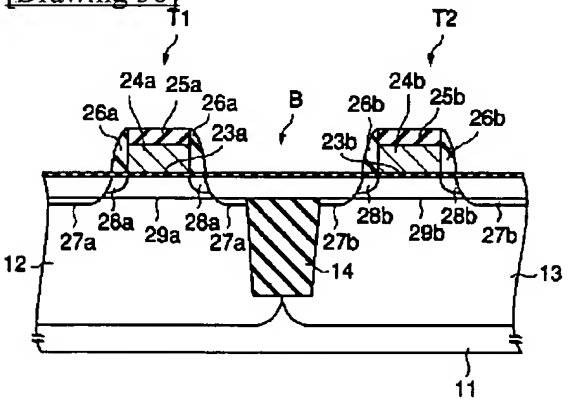

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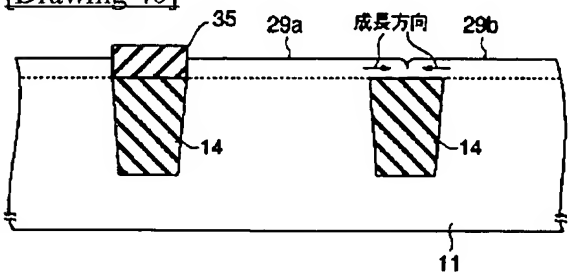

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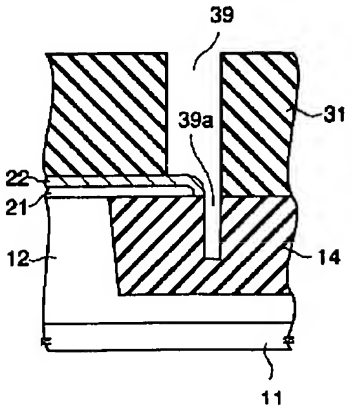

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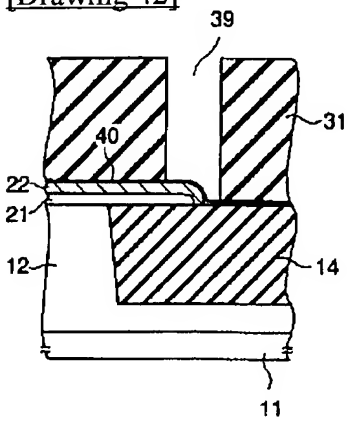

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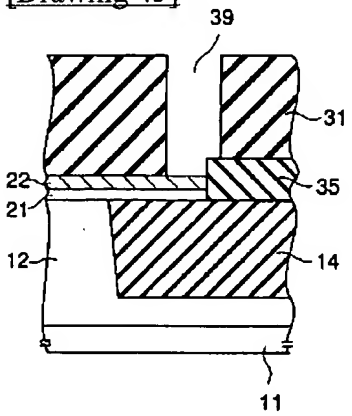

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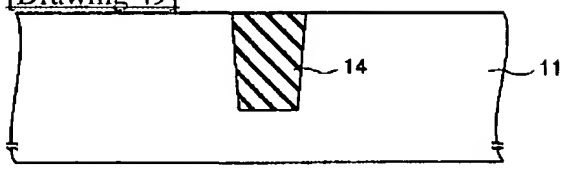

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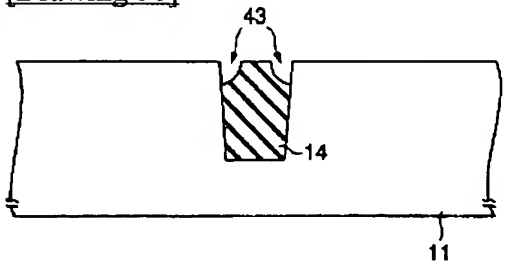

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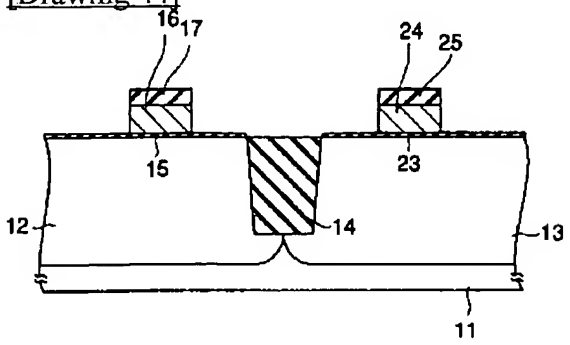

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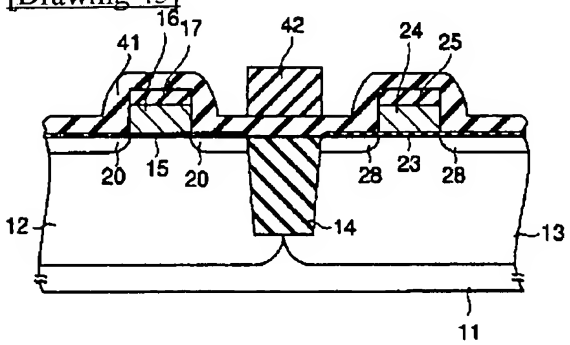

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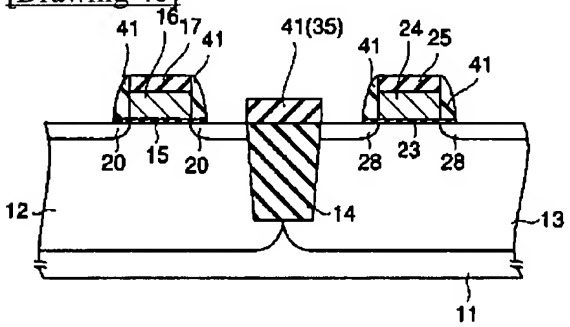

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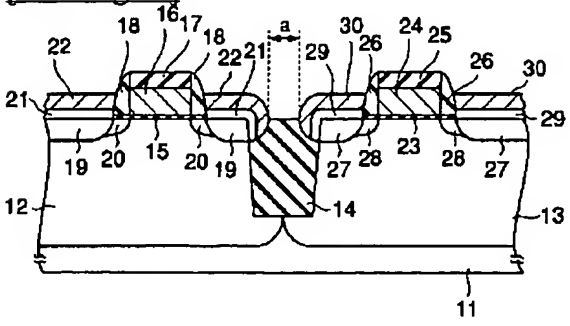

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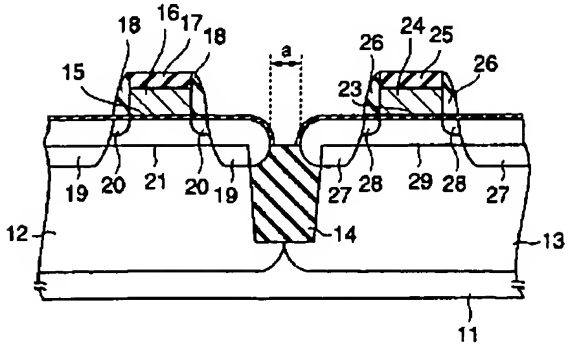

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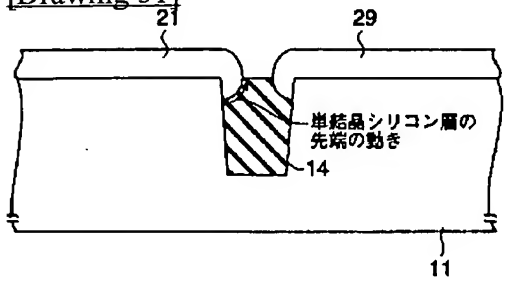

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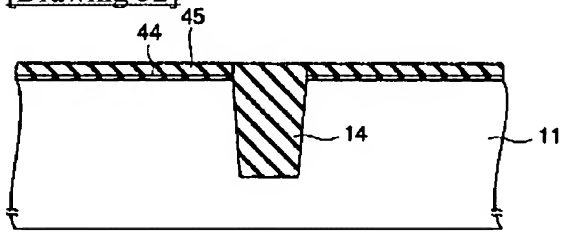

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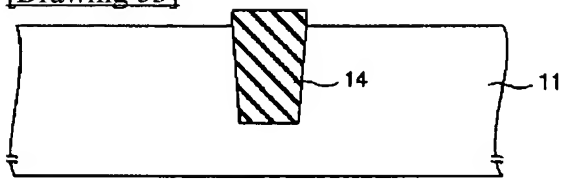

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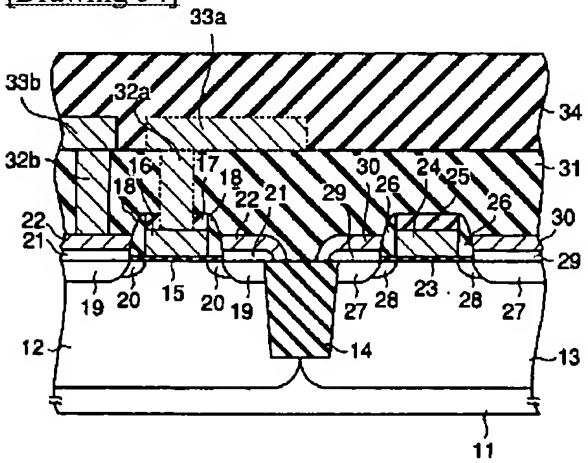

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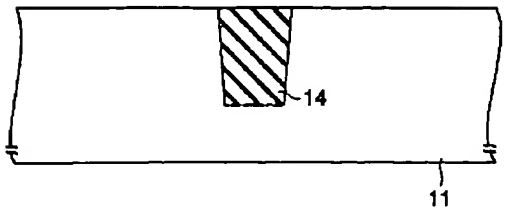

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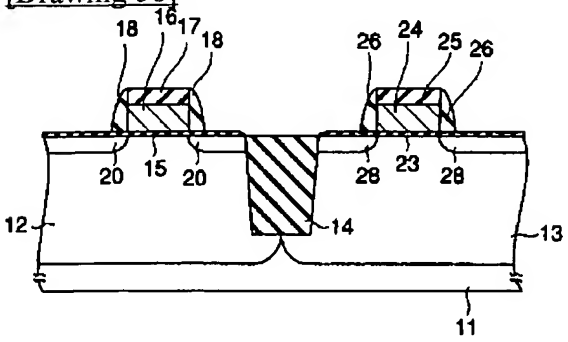

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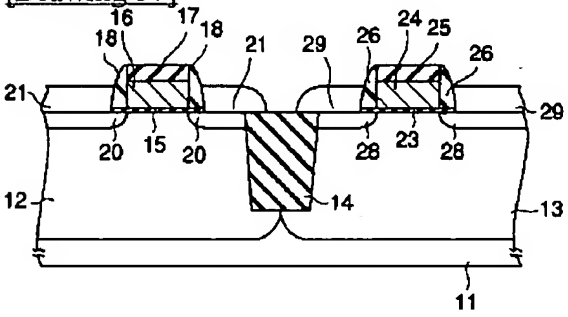

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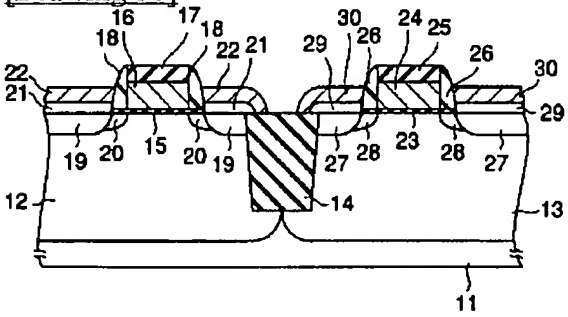

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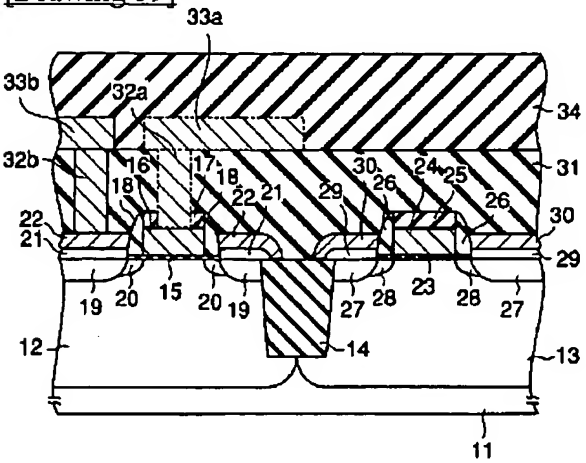

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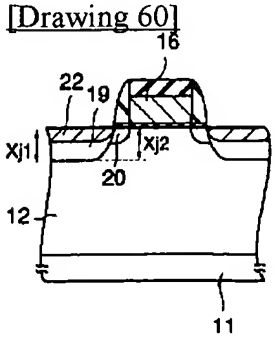

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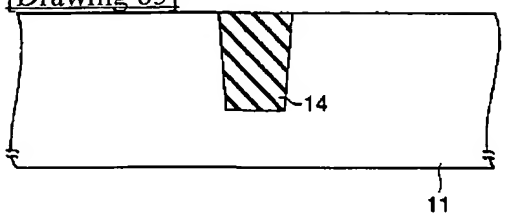

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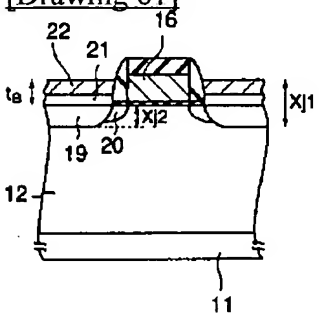

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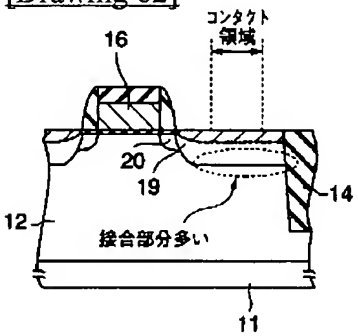

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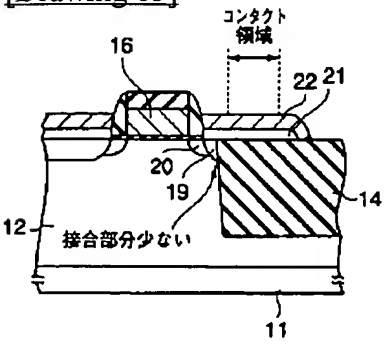

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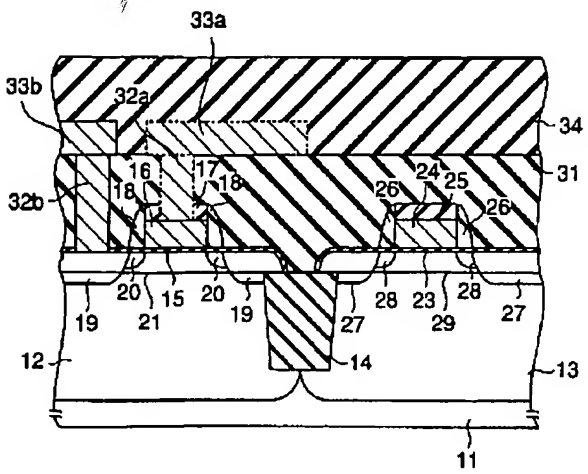

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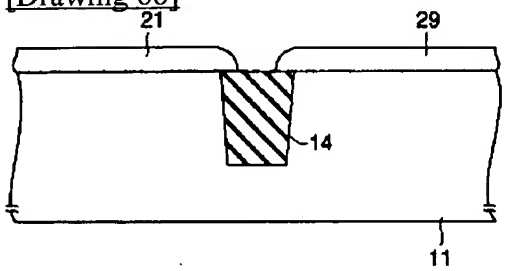

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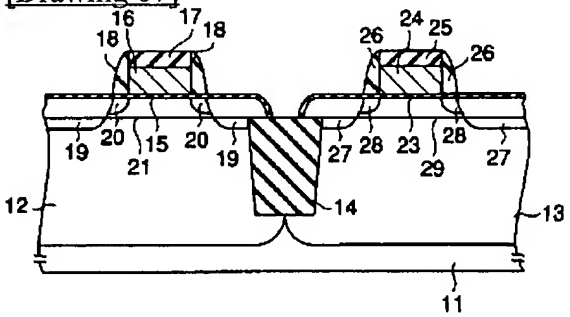

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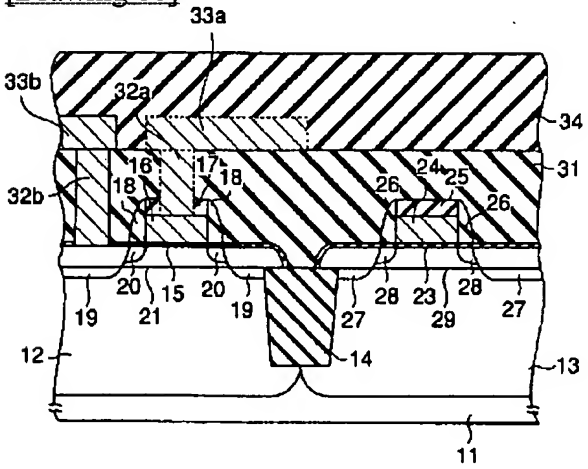

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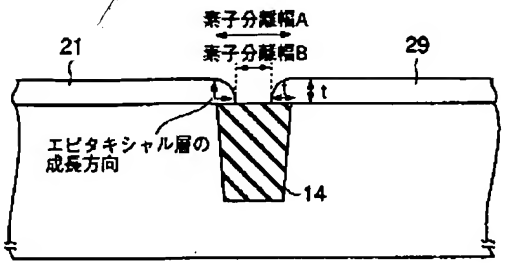

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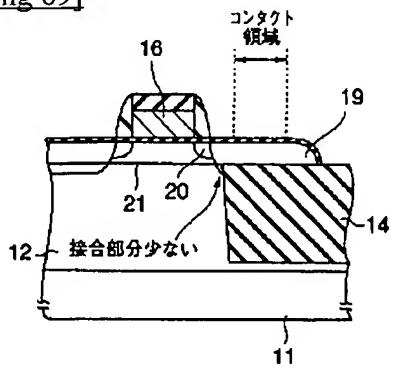

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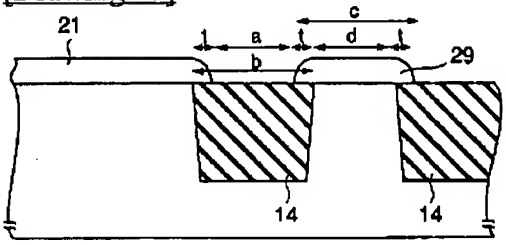

[Translation done.]